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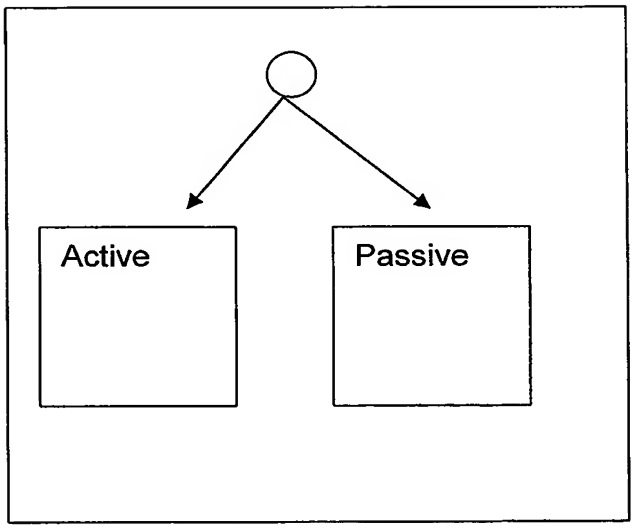


Figure 1 Traffic Node System Description

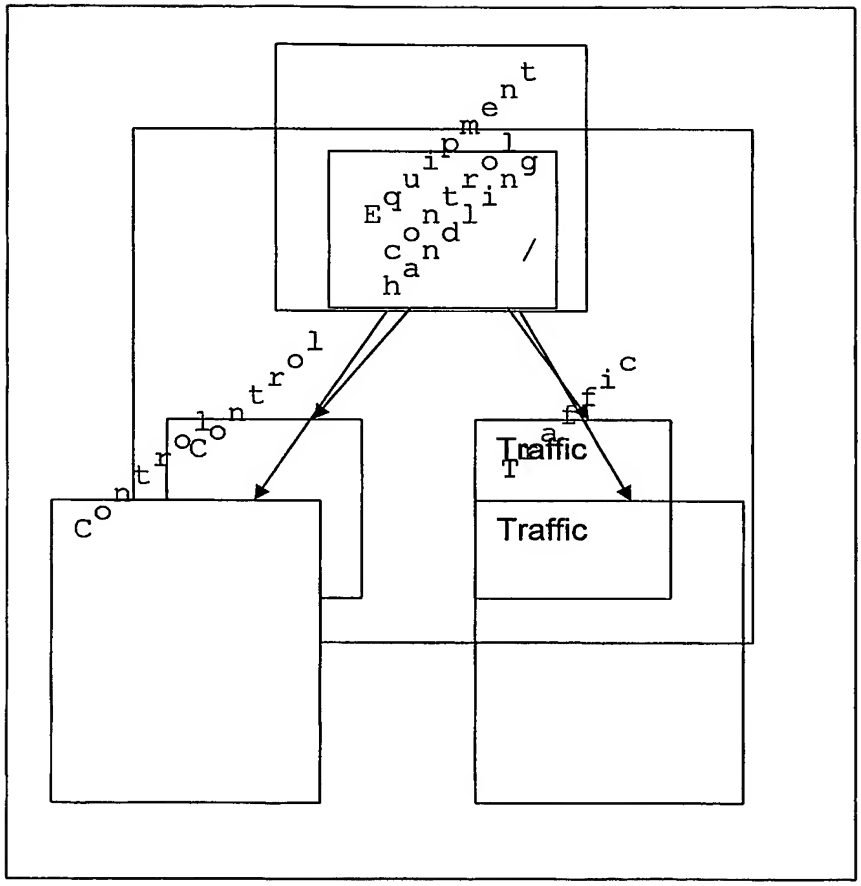


Figure 2 Application of the Traffic Node in the Lower Radio Access Network

2

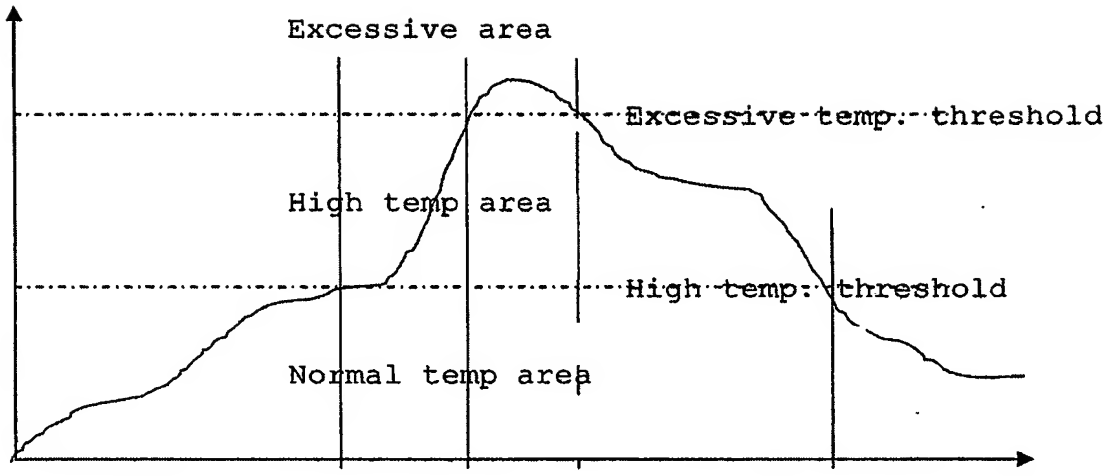


Figure 3 LRAN network and the role of various Traffic Node sub-networks.

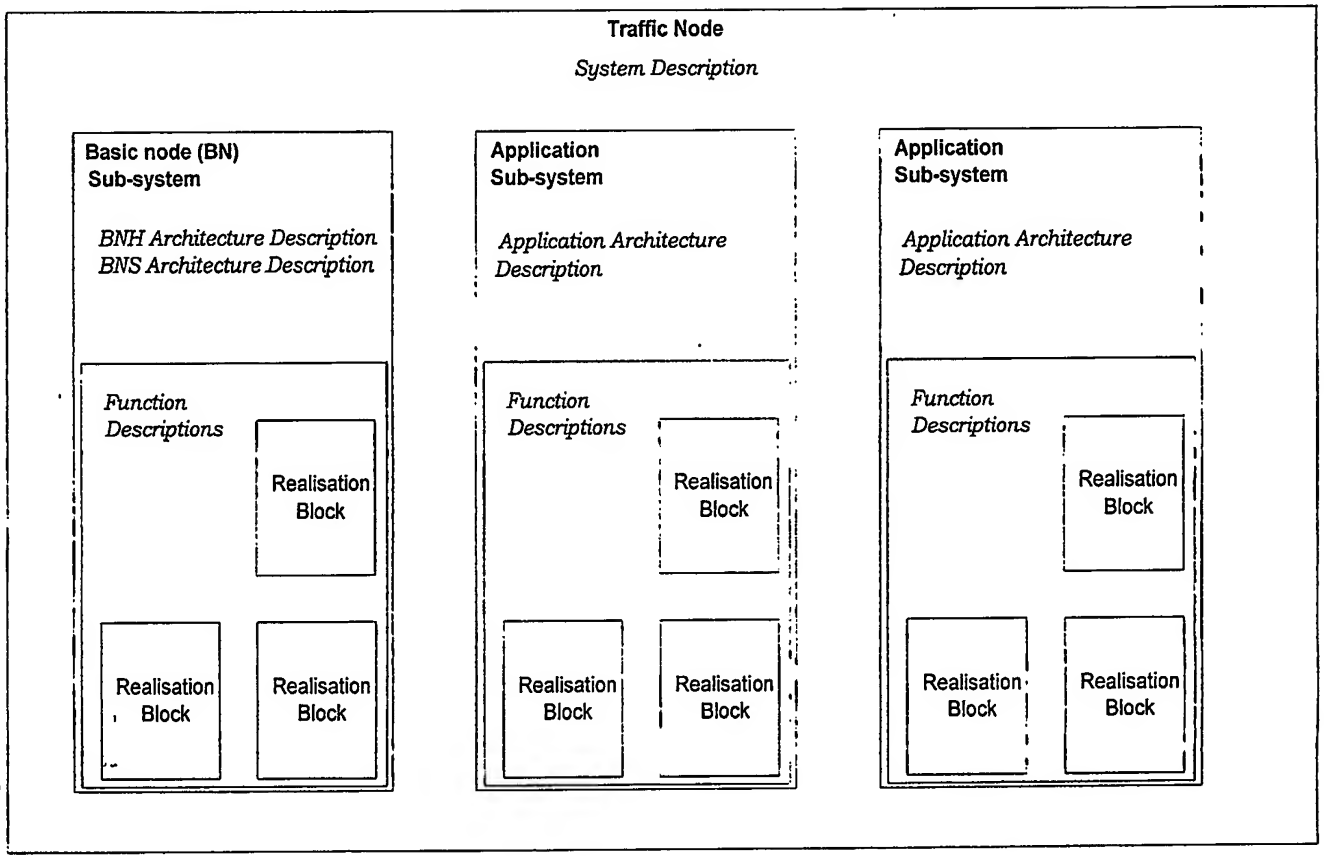


Figure 4 O&M environment of Traffic Node

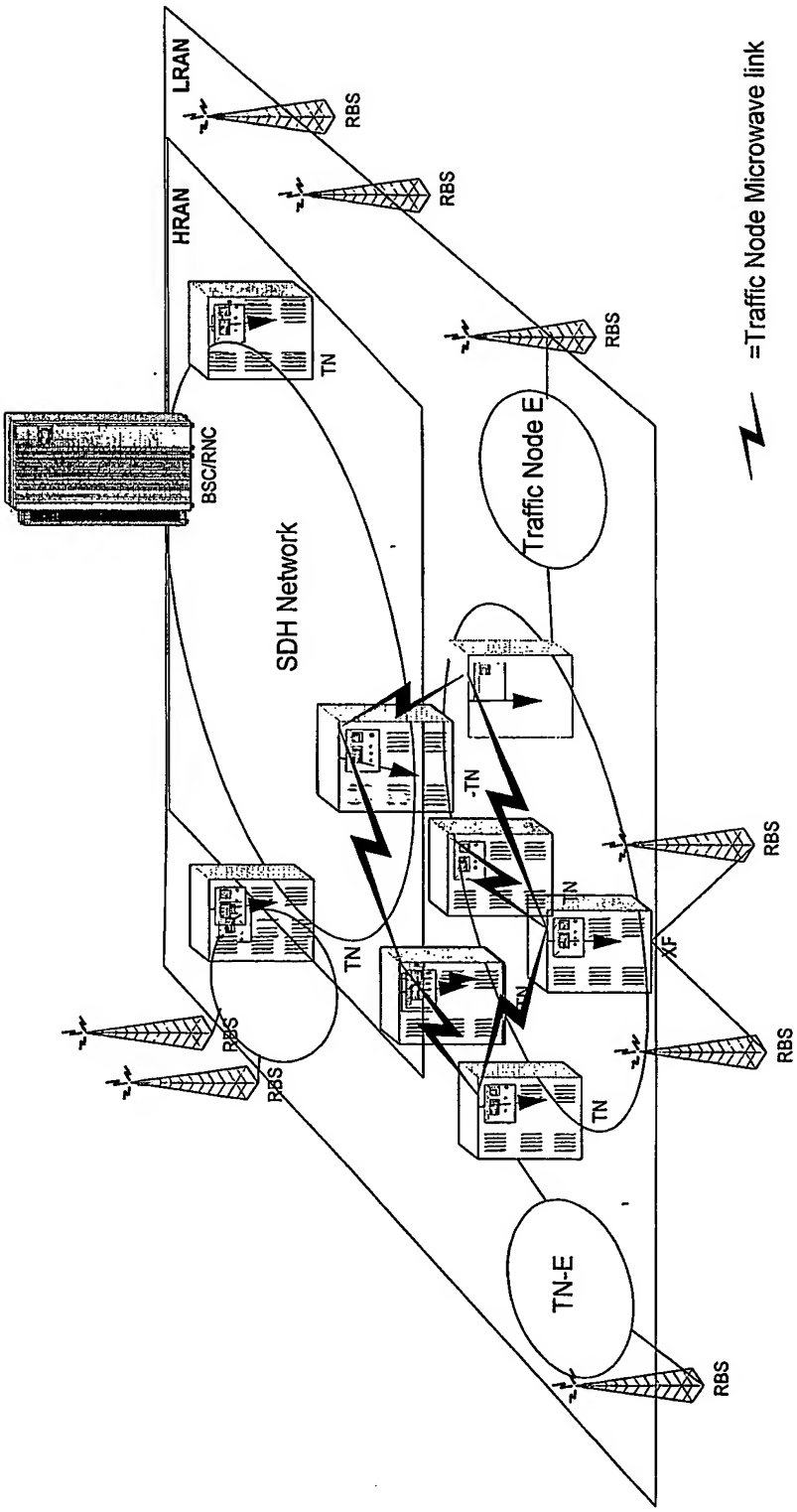


Figure 5 The TN IP based DCN

5

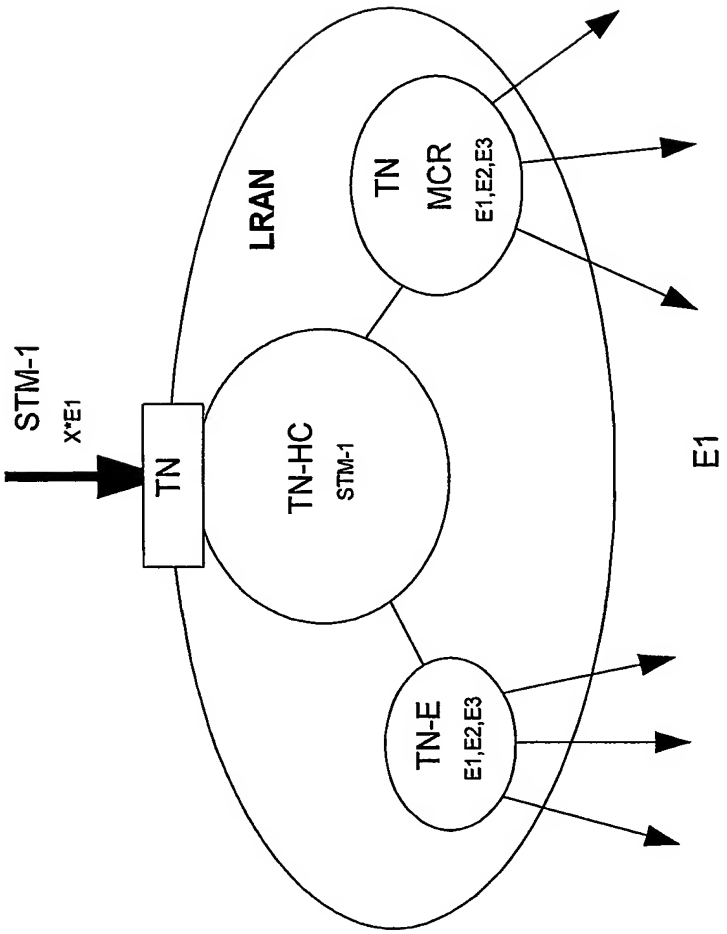


Figure 6 TN modularity

6

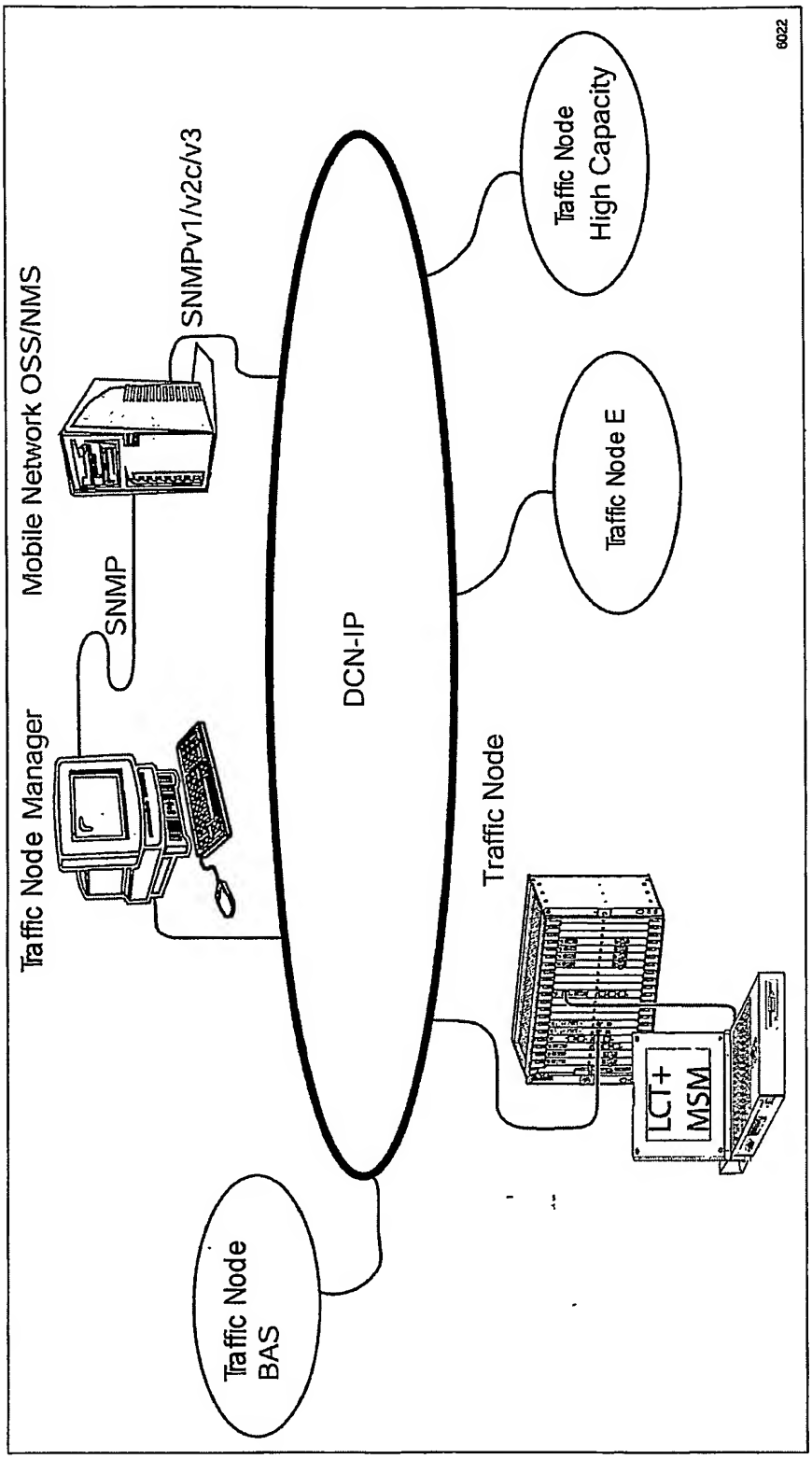


Figure 7 TN architecture

7

8

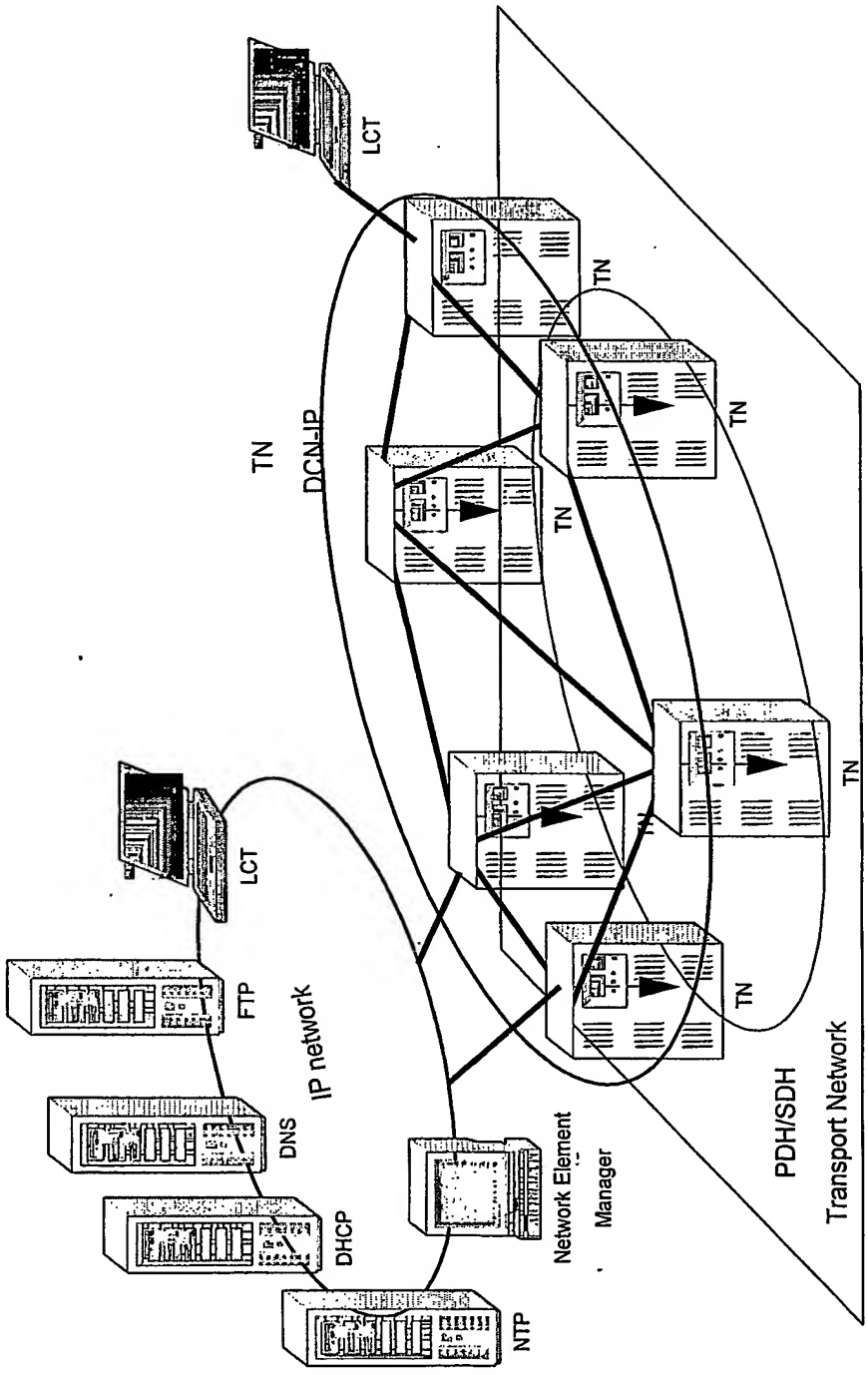


Figure 8 TN software architecture

9

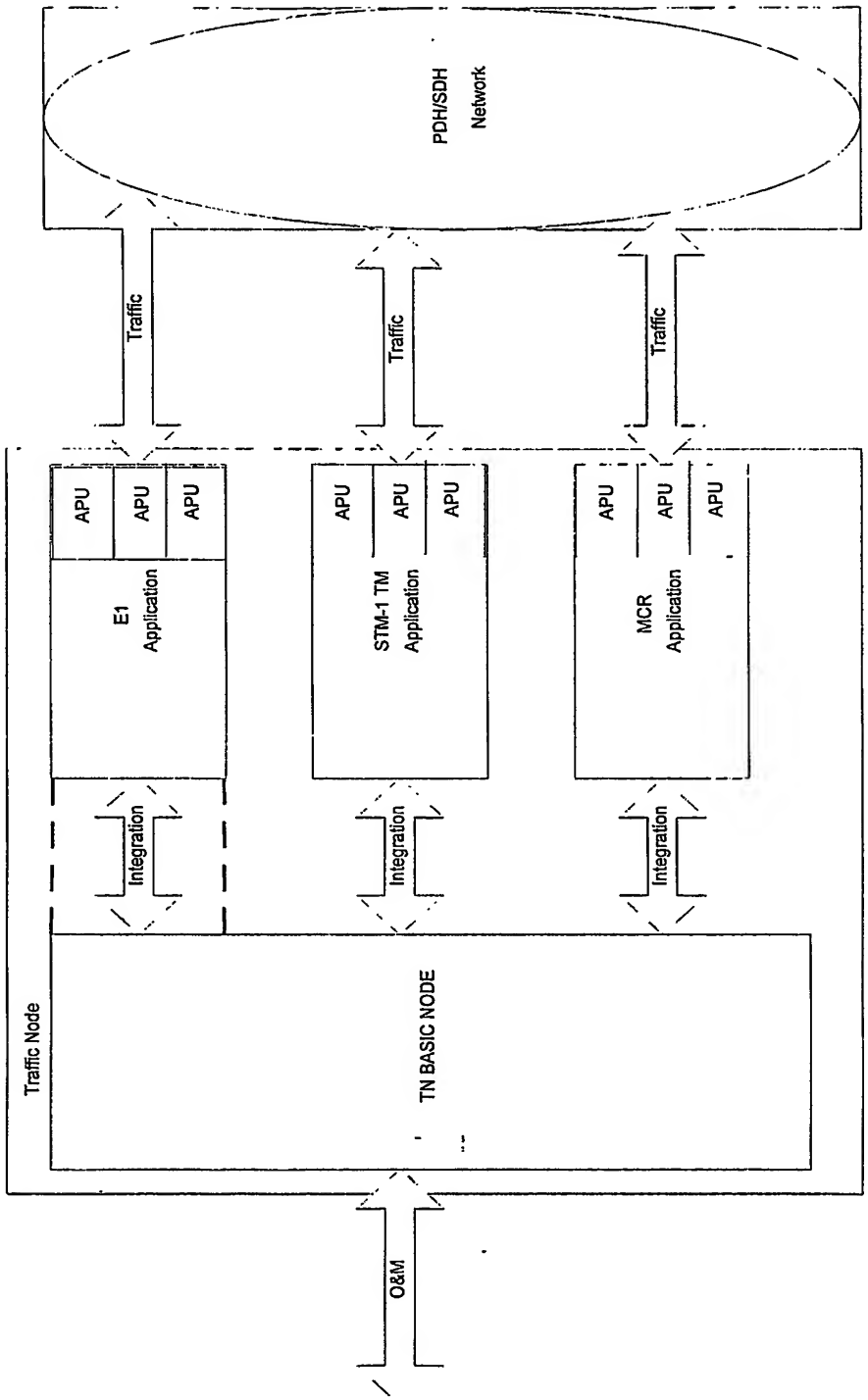
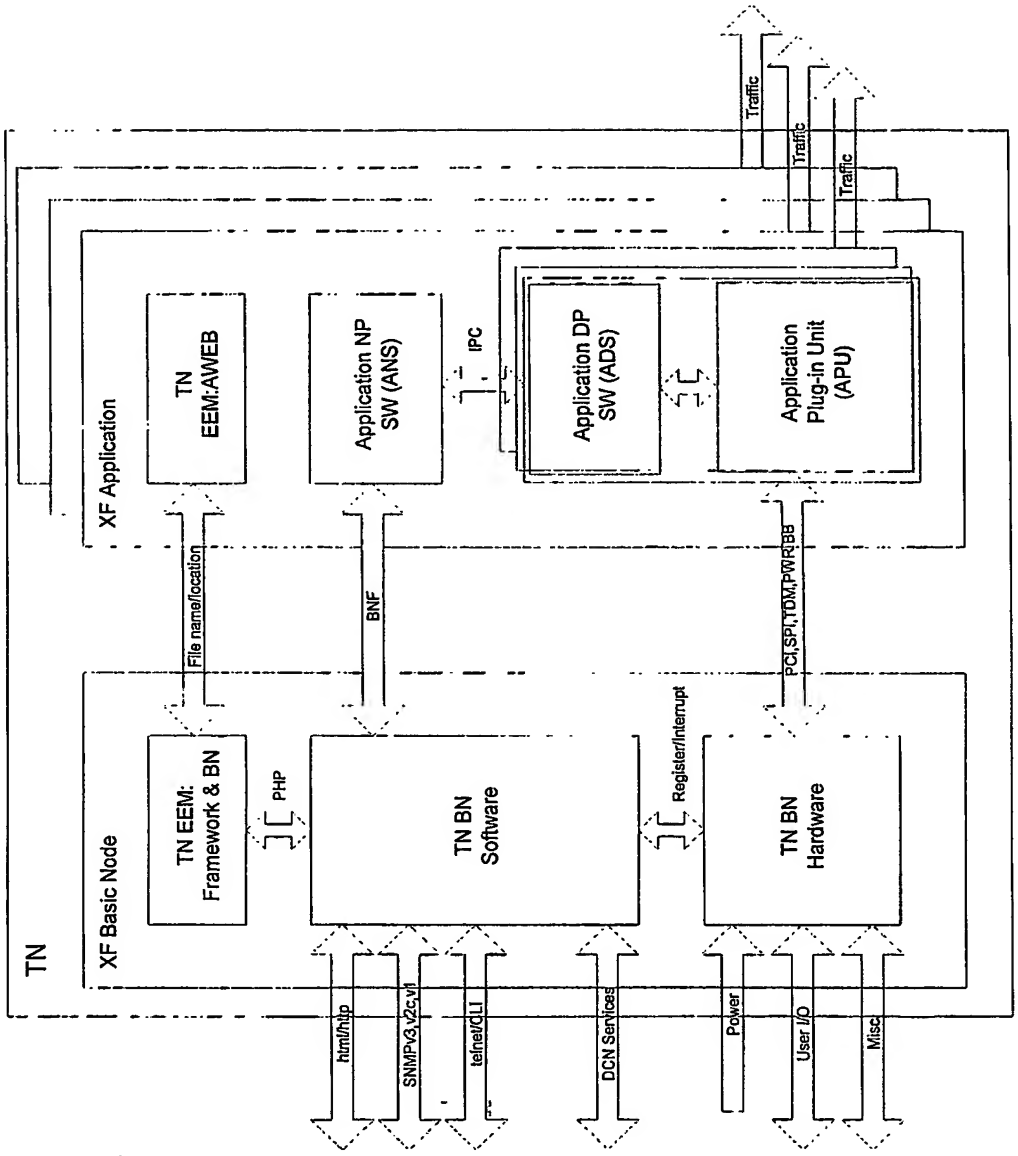


Figure 9 TN BNH busses and building blocks



10

Figure 10 The TN AMM 20p Backplane

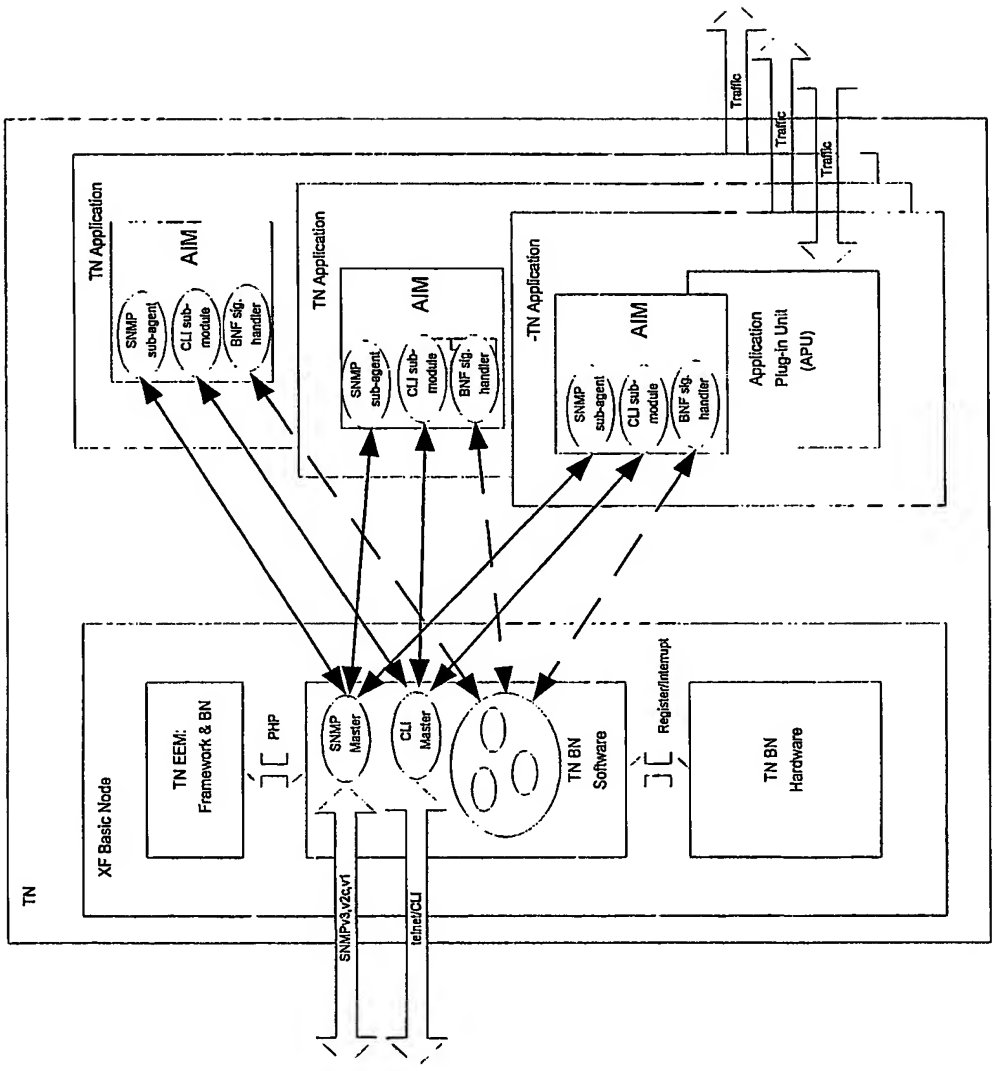


Figure 11 TN BNS

11

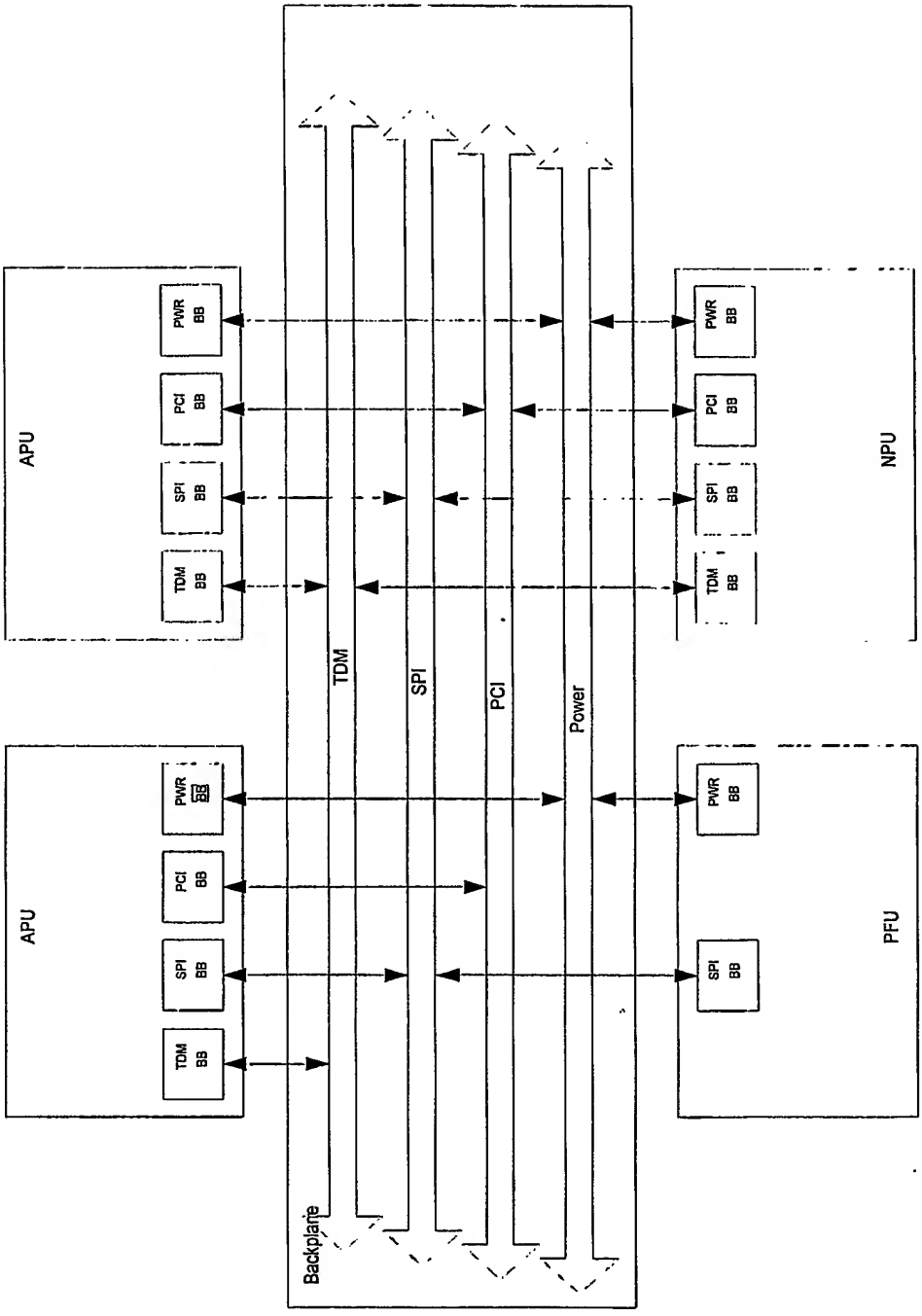


Figure 12 TN EEM: Framework and Basic Node

12

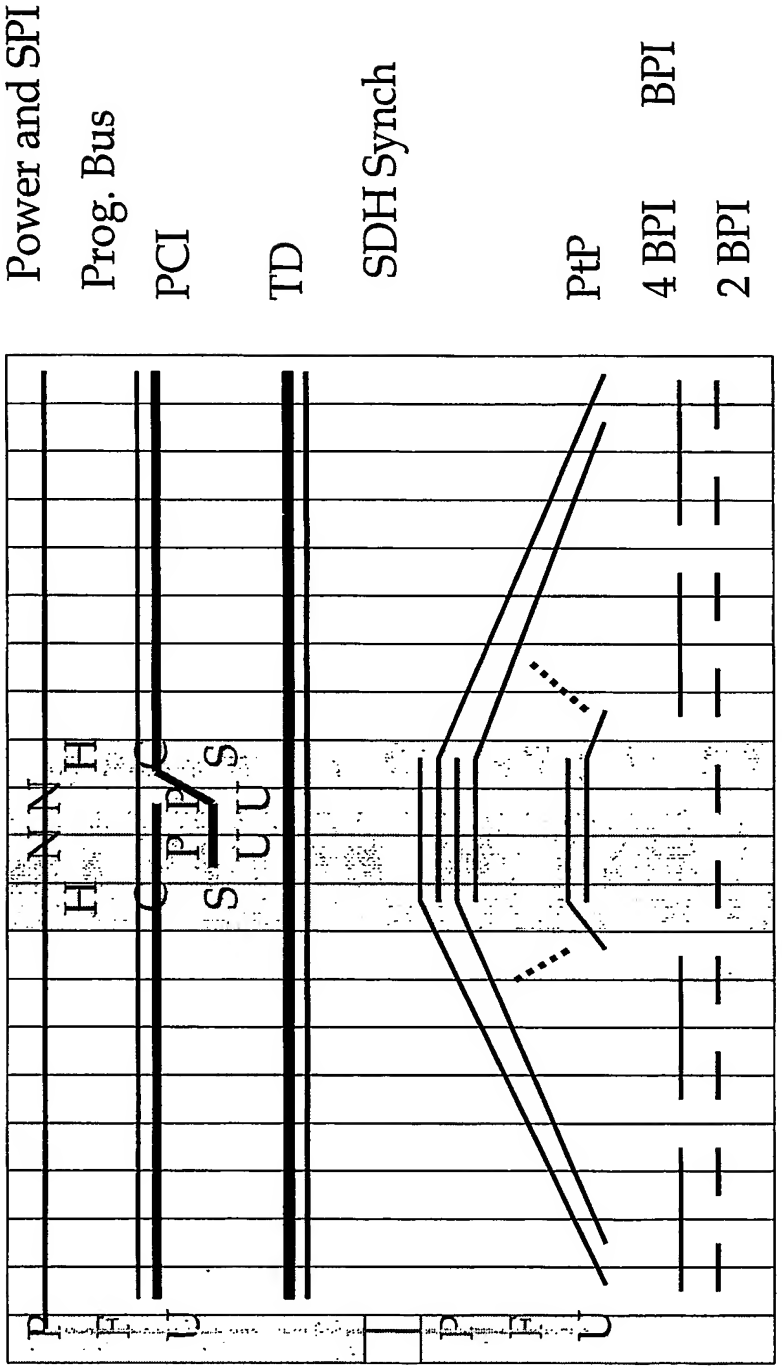


Figure 13 TN BNH

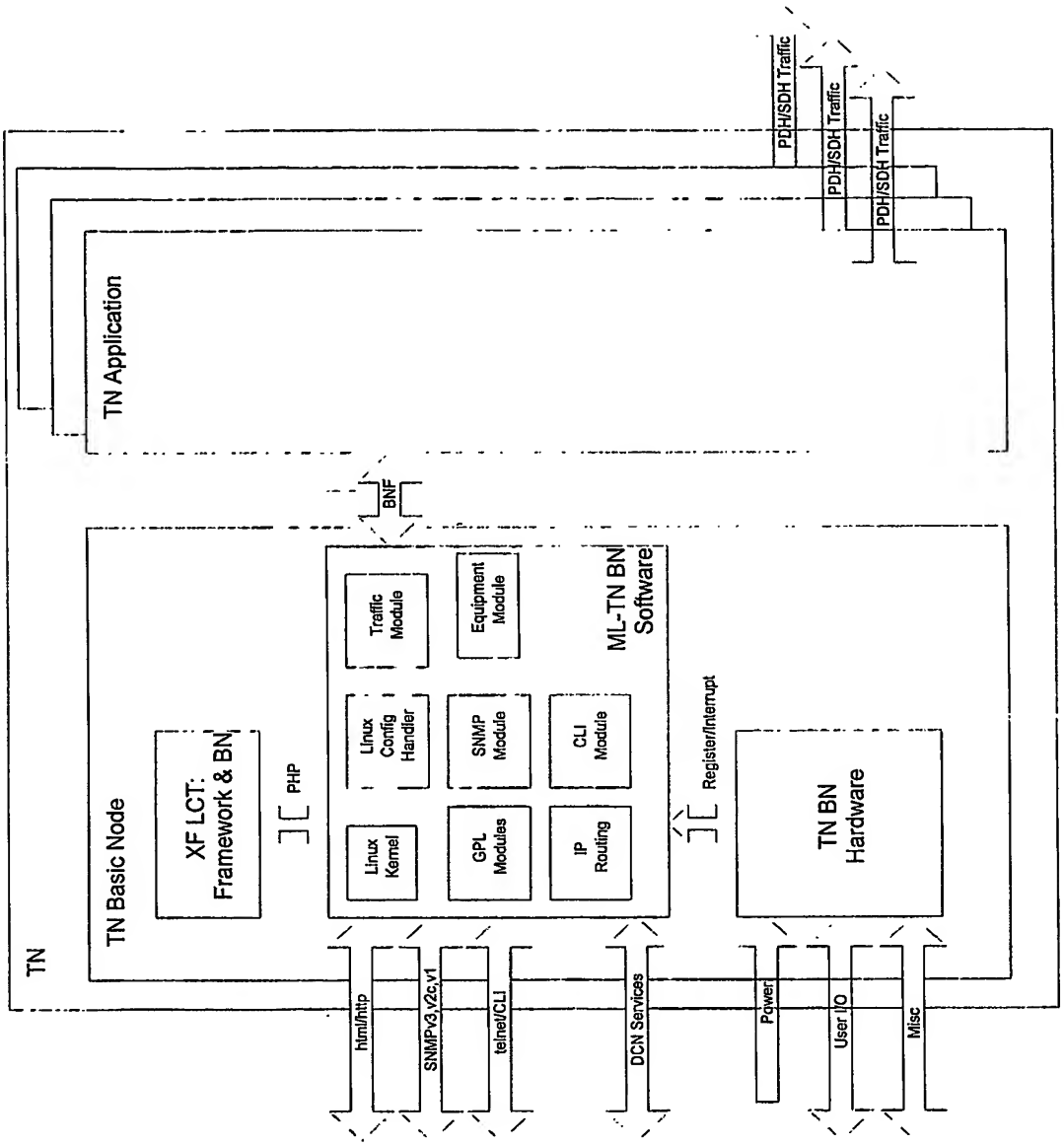


Figure 14 TN Application architecture

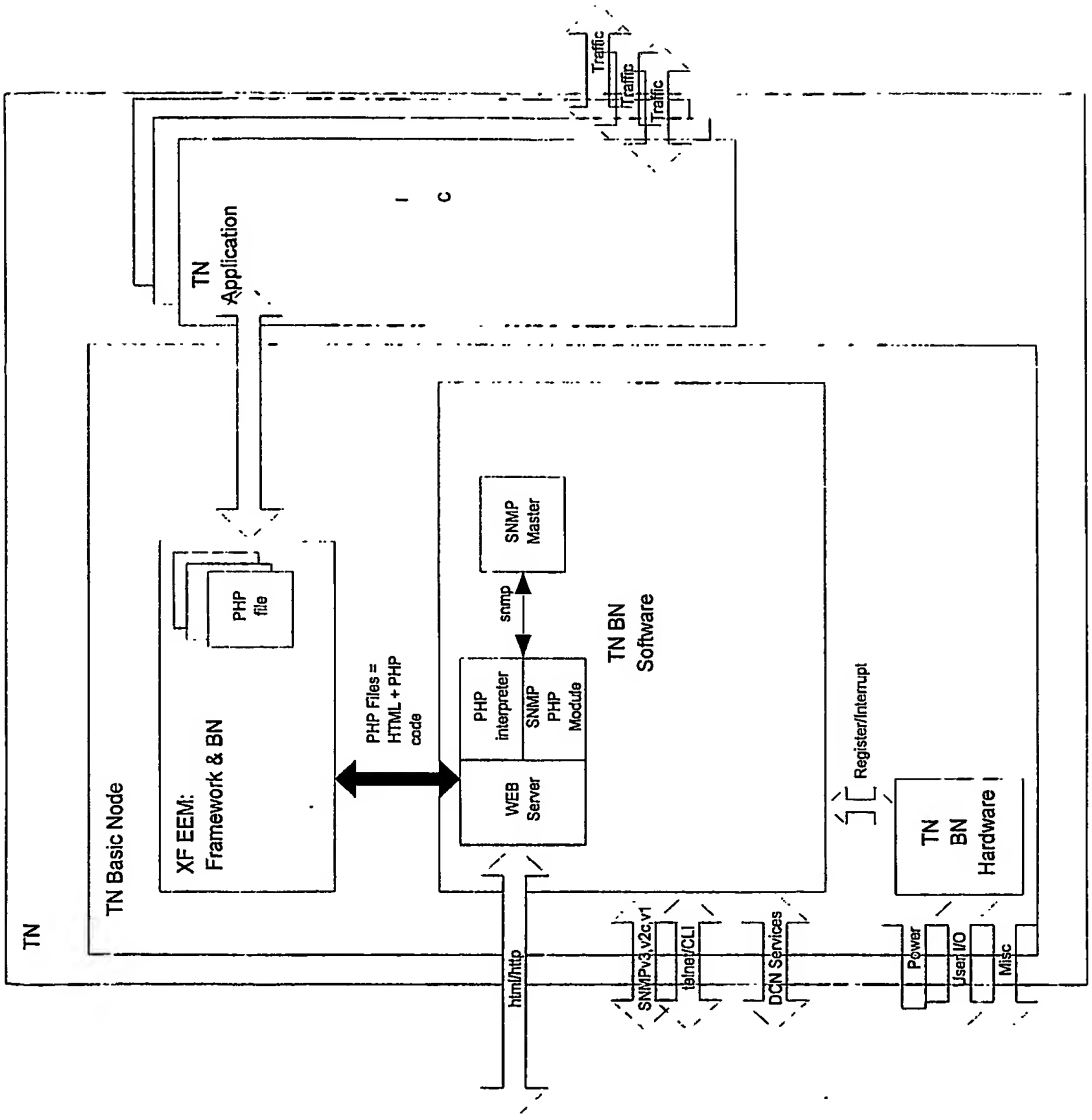


Figure 15 TN Application Software

15

16

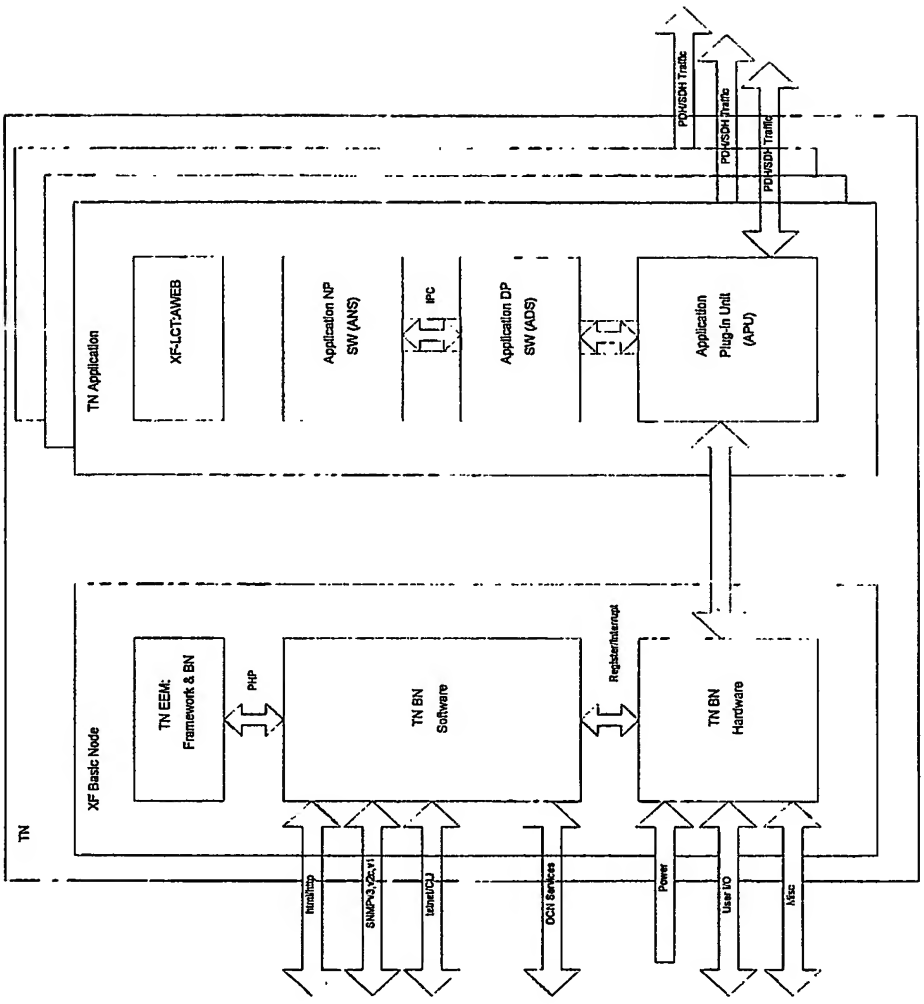


Figure 16 TN ANS architecture

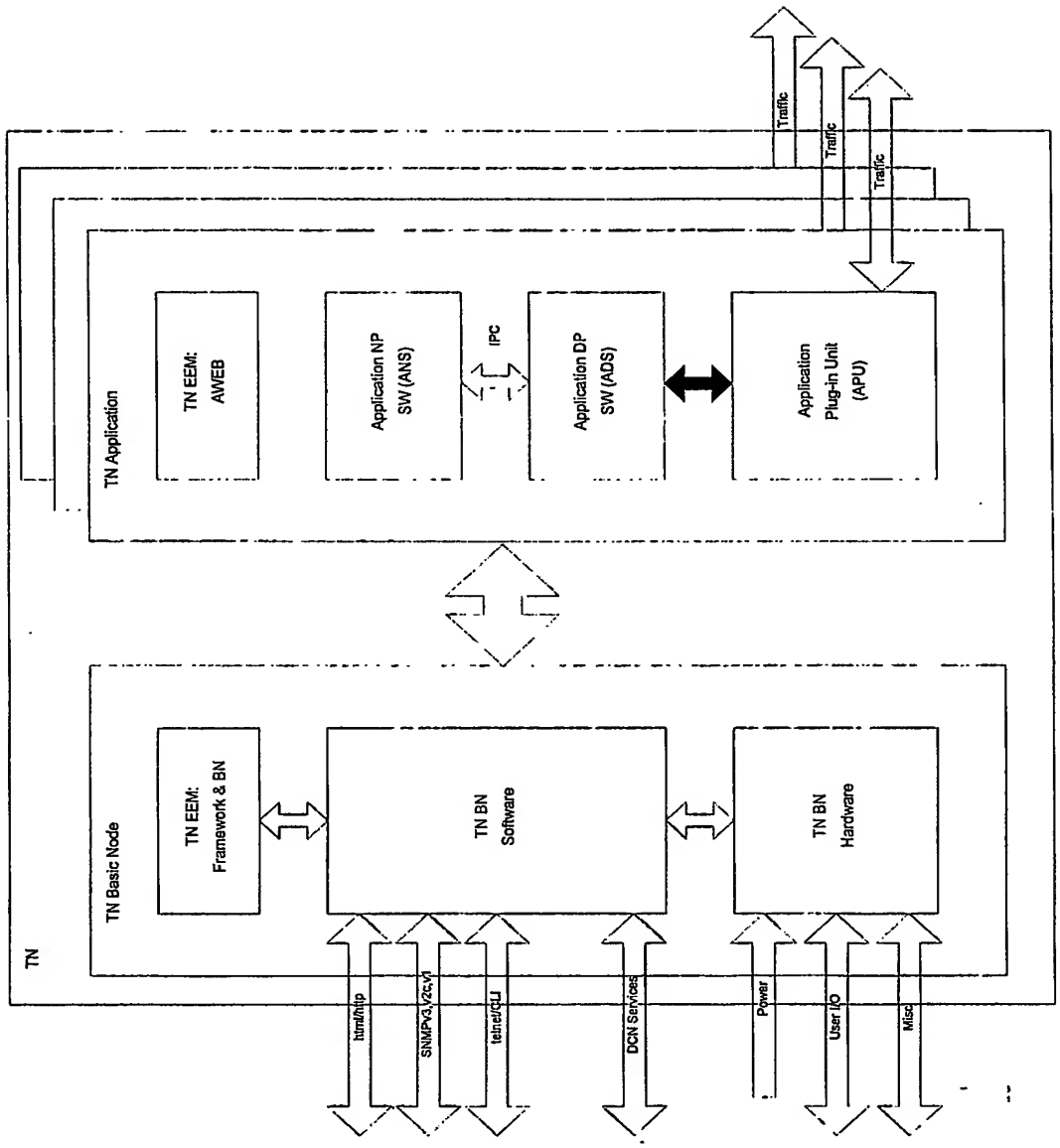


Figure 17 TN Application EEM

17

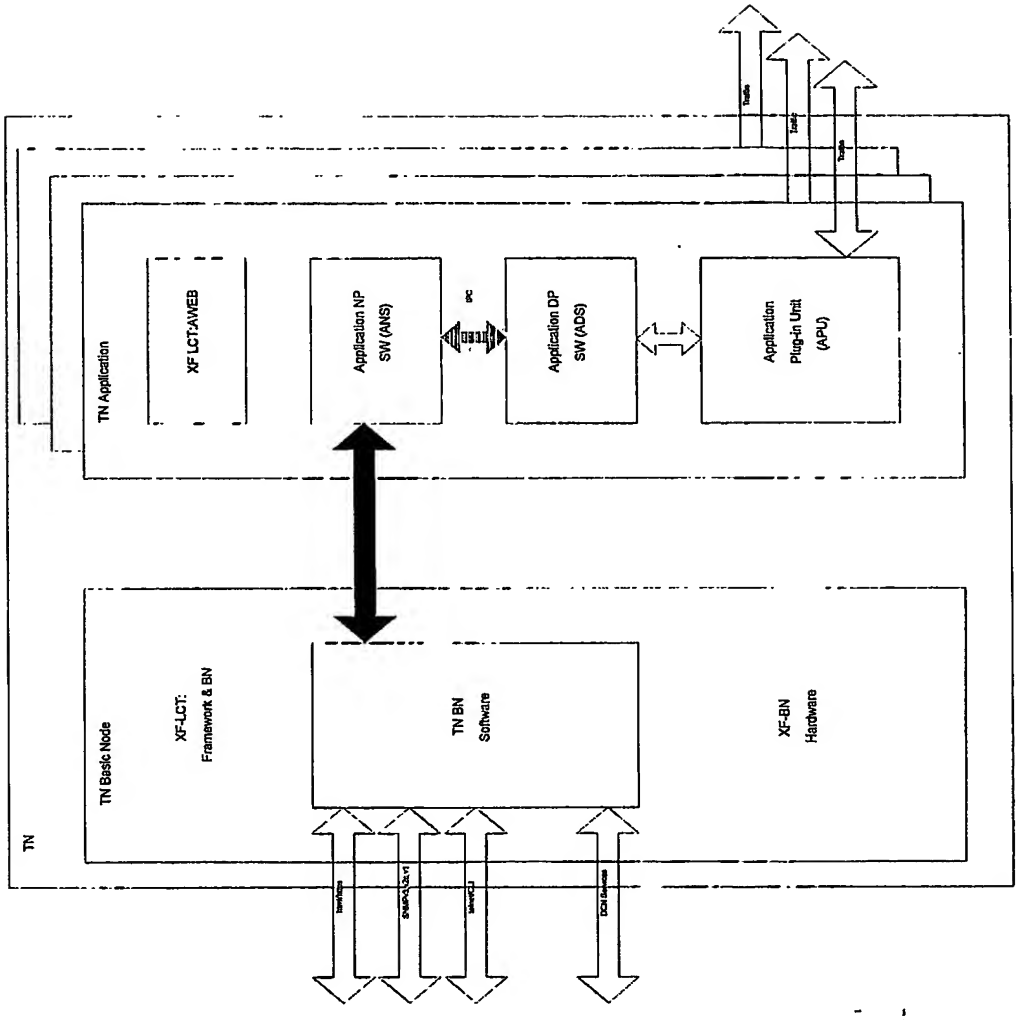


Figure 18 TN Application Hardware

18

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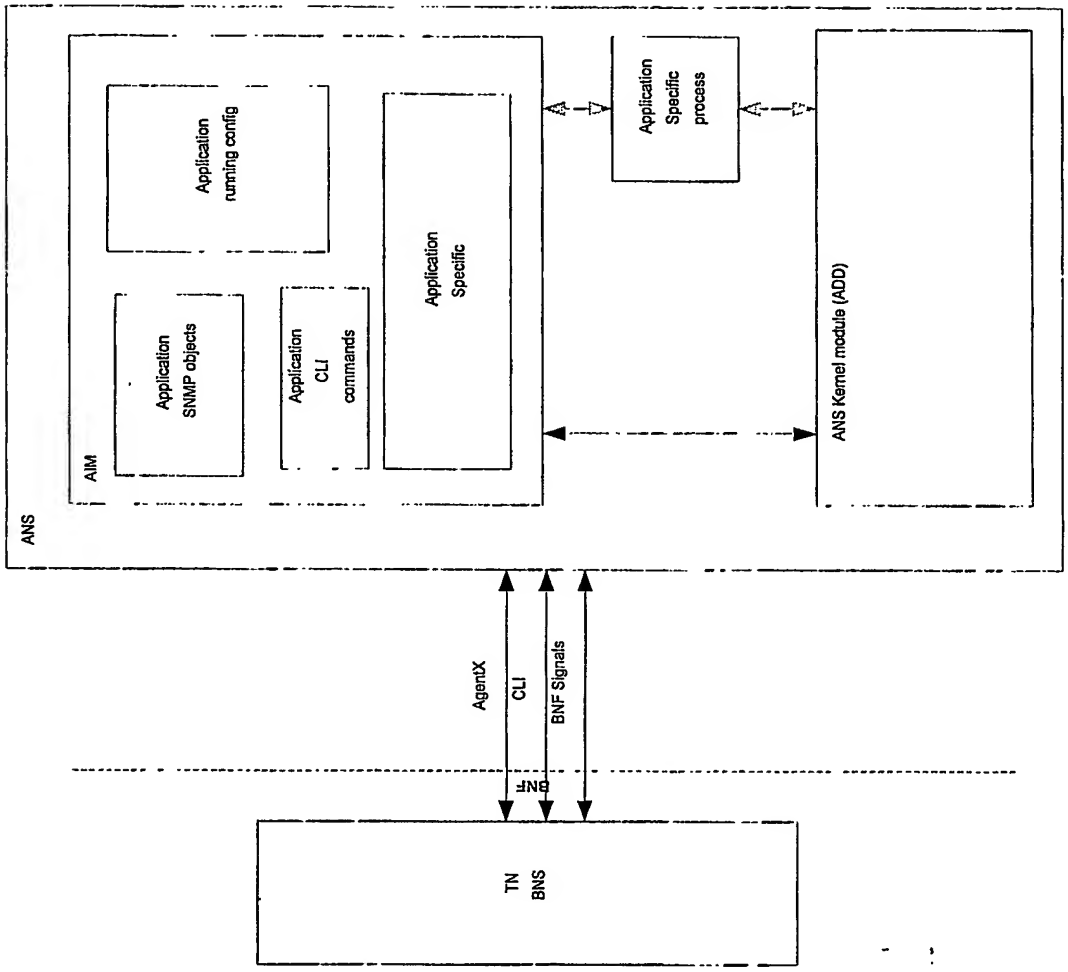


Figure 19 TN APU

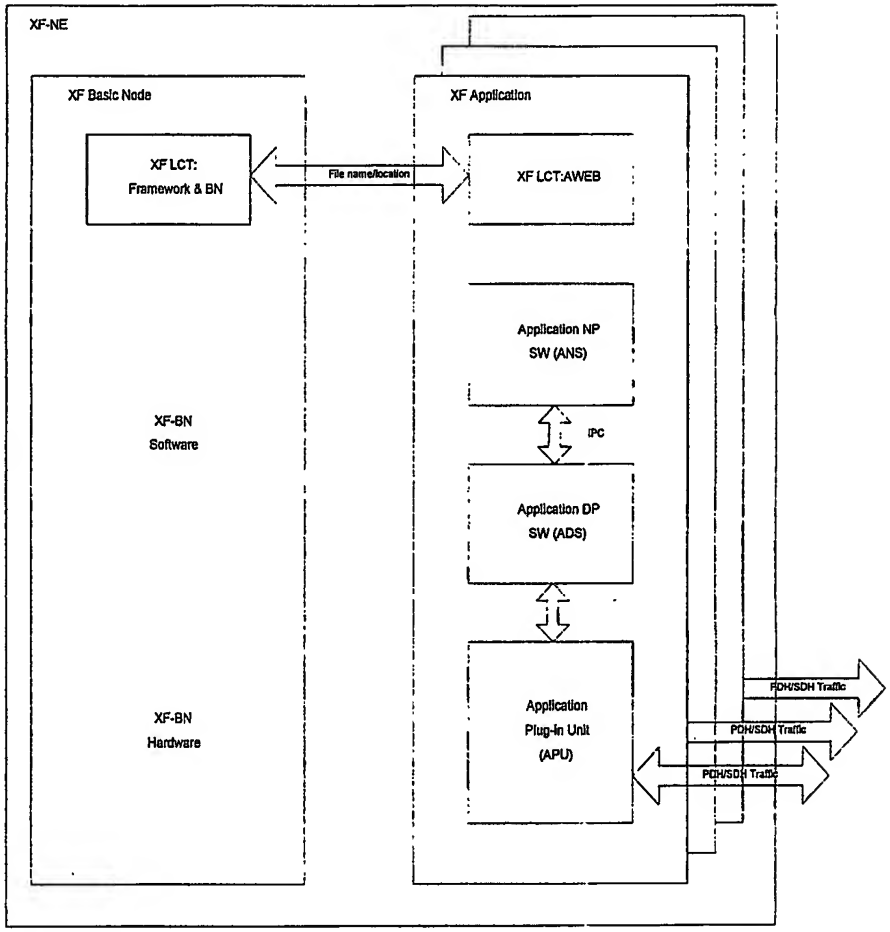


Figure 20 Example of a bi-directional 3*64Kbs cross-connection between the two APUs

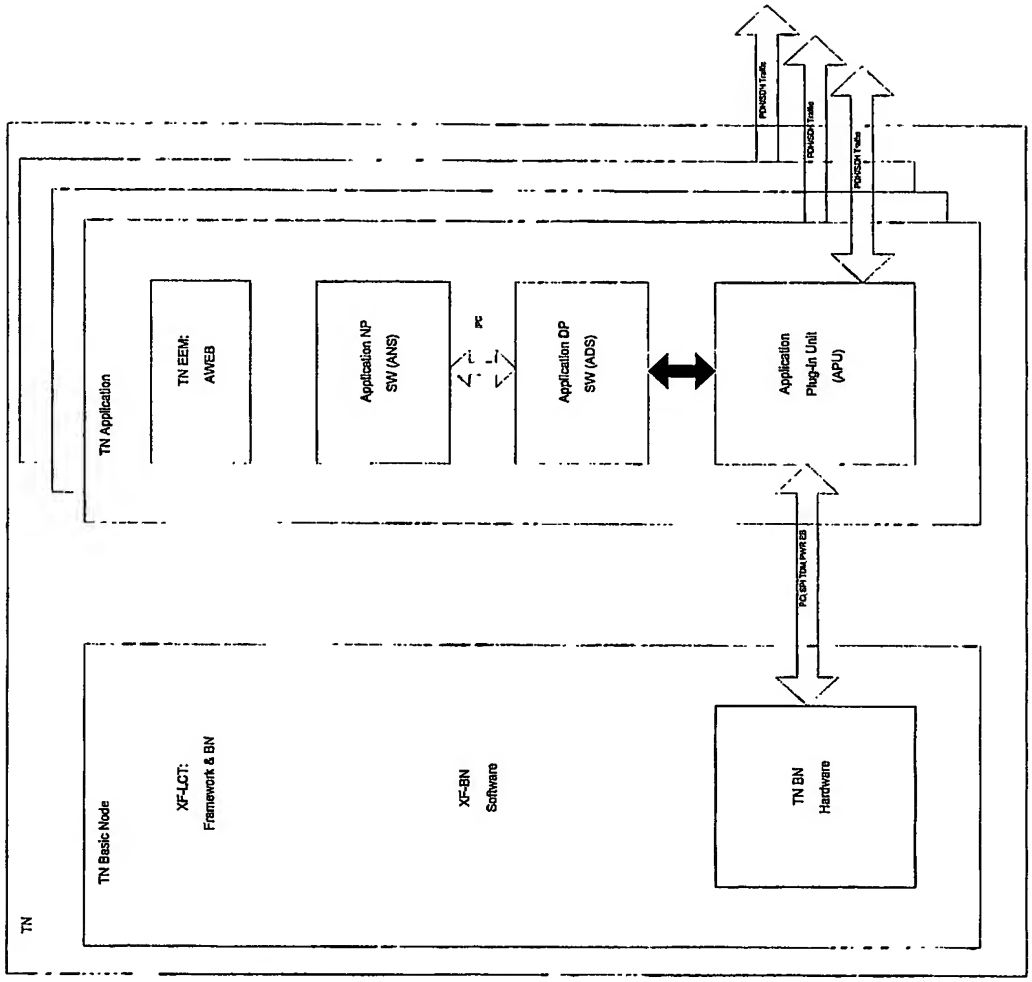


Figure 21 PM handling in TN

21

22

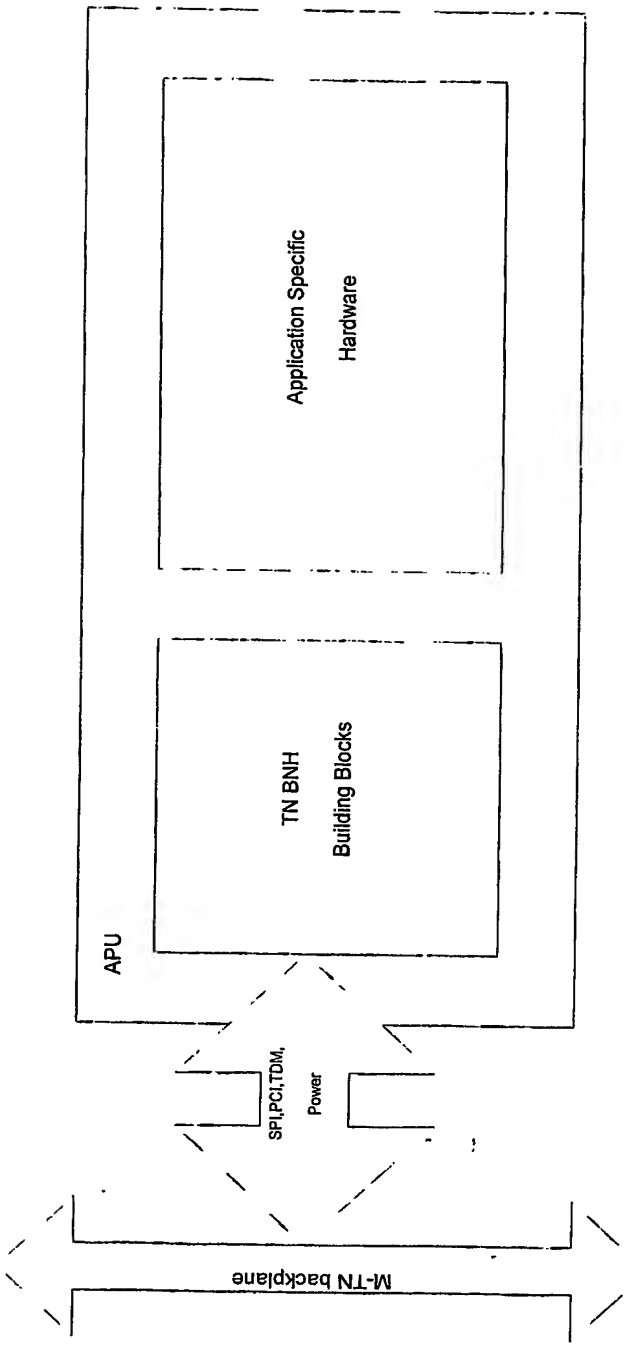


Figure 22 TN Alarm Handling overview

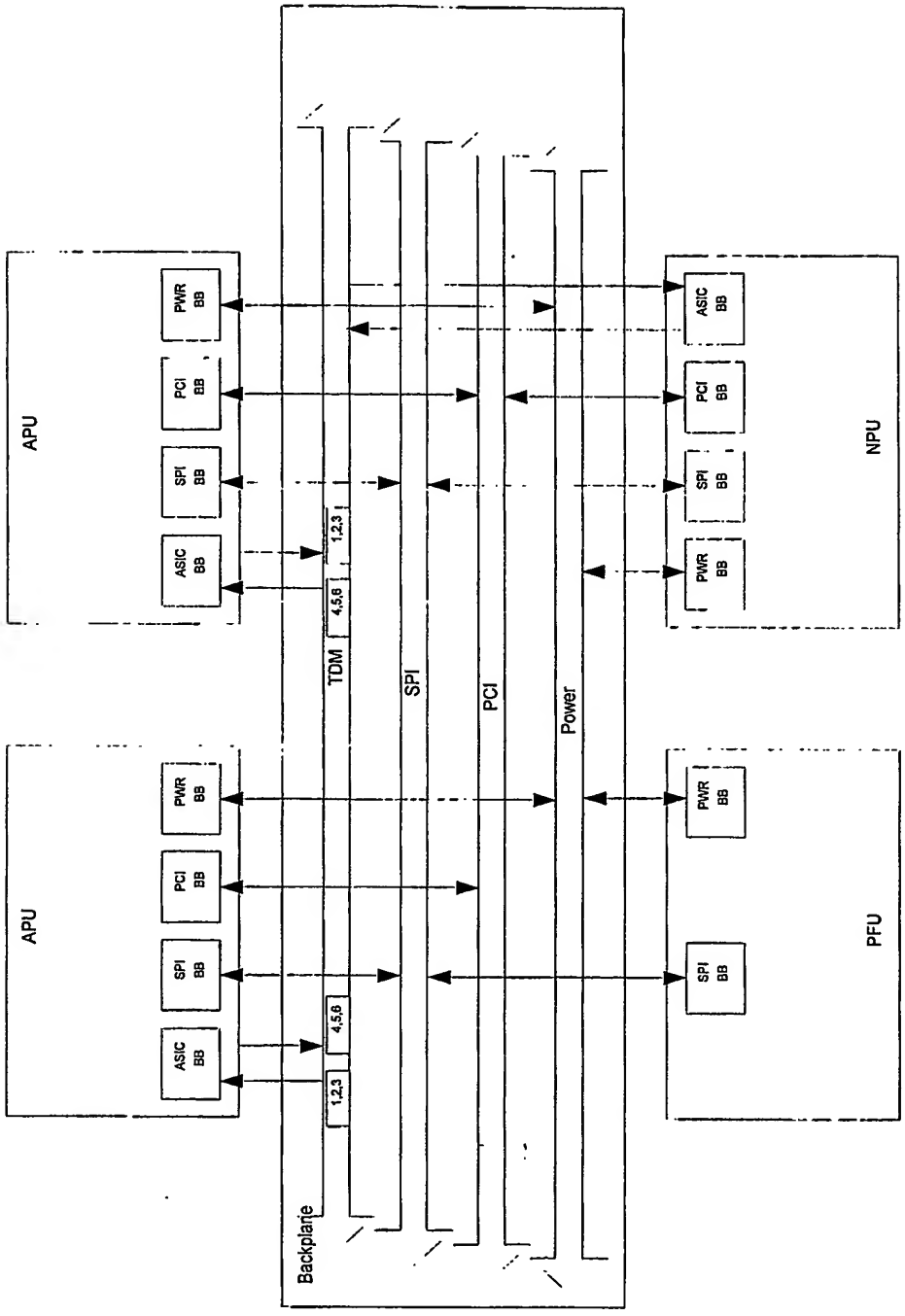


Figure 23 E1 carried on one interface.

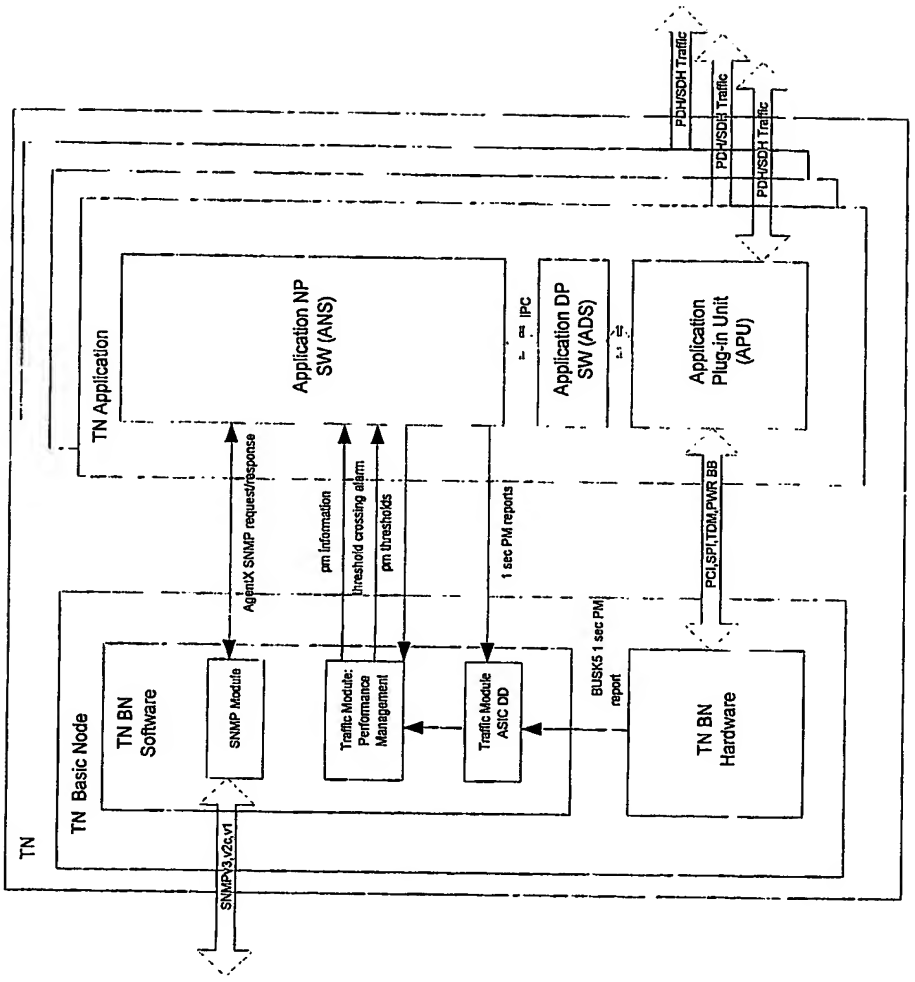


Figure 24 E1 carried on a terminal

BNS and ANS uses BNF messages.

24

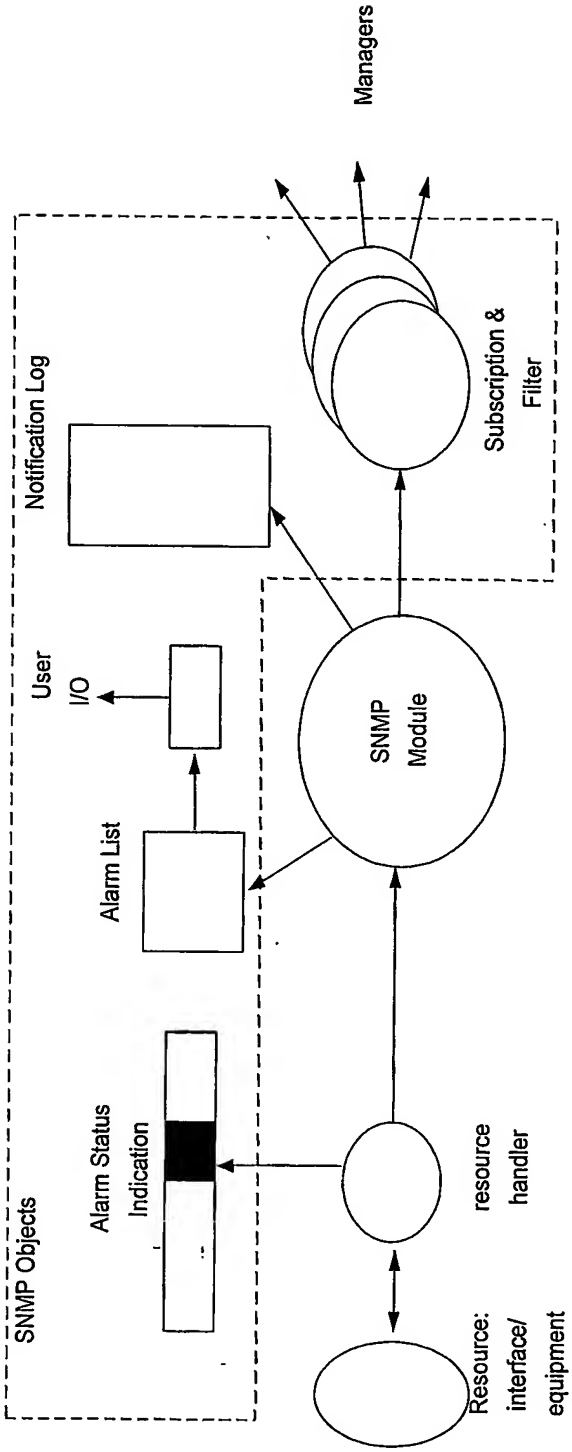


Figure 25 Redundancy model - basis for calculations

25

26

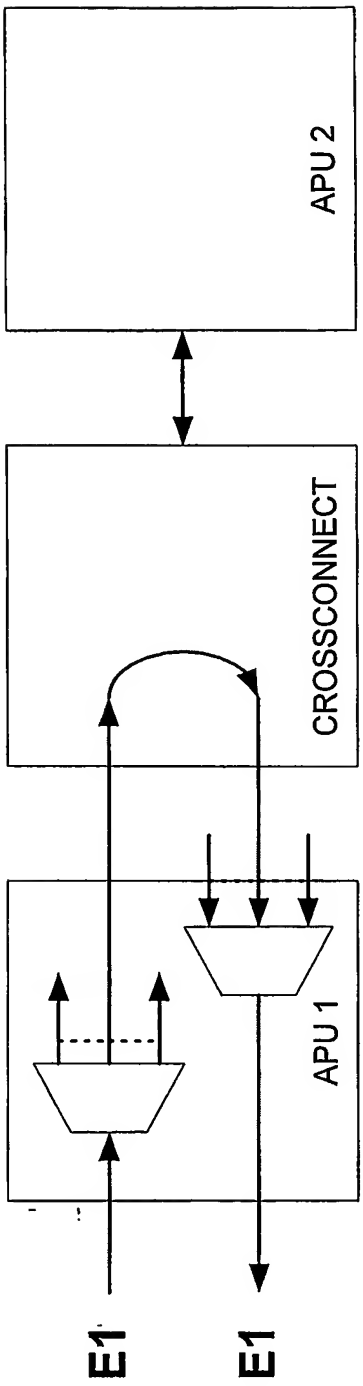


Figure 26 PIU function blocks

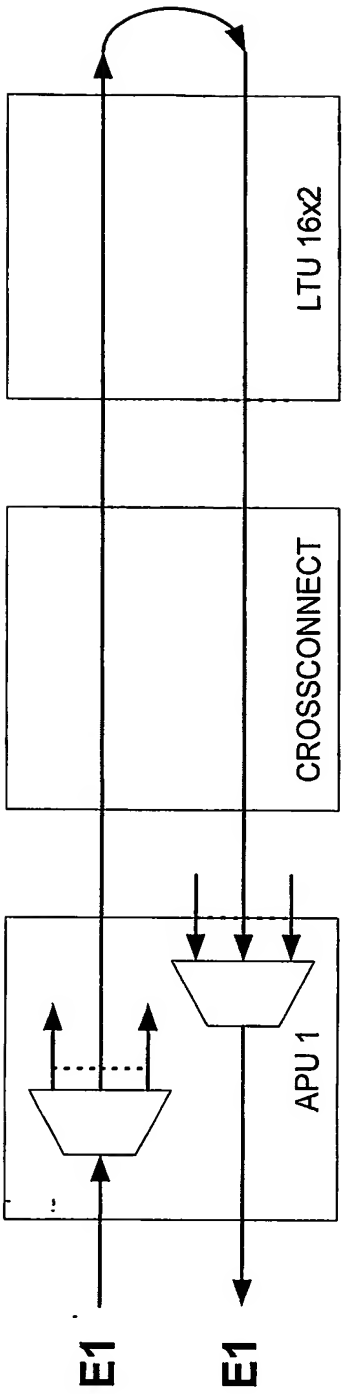


Figure 27 ASIC block structure

28

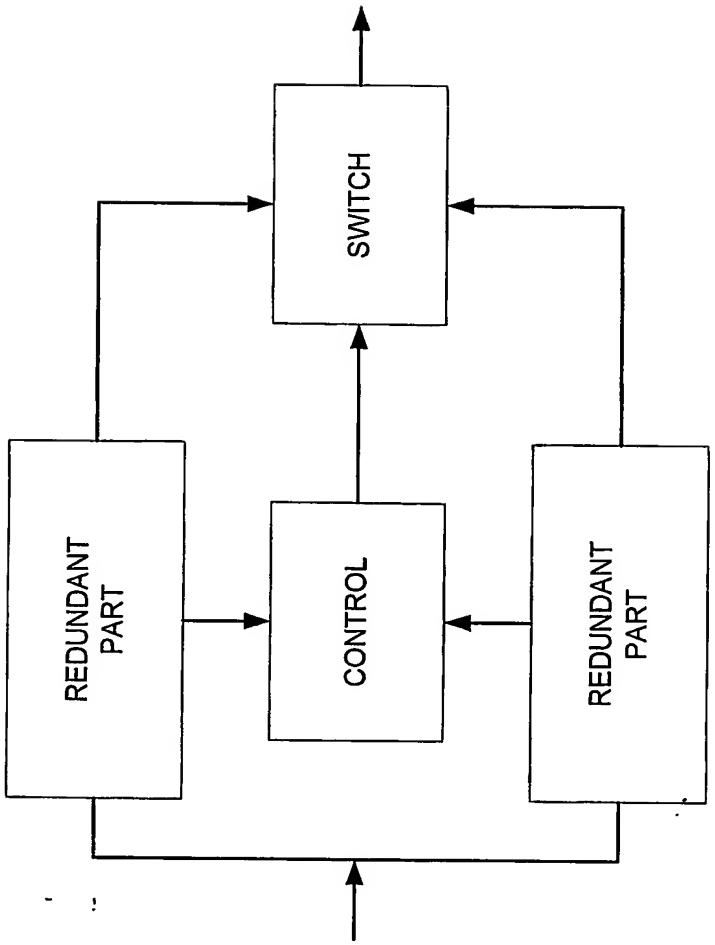


Figure 28 TDM bus redundancy

29

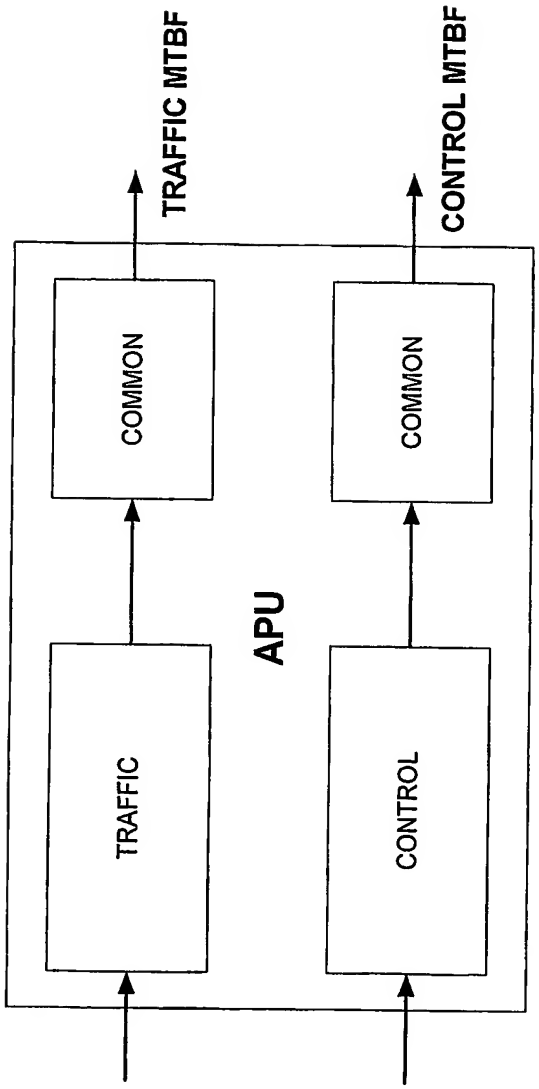


Figure 29 AMM 20p with redundant power distribution

30

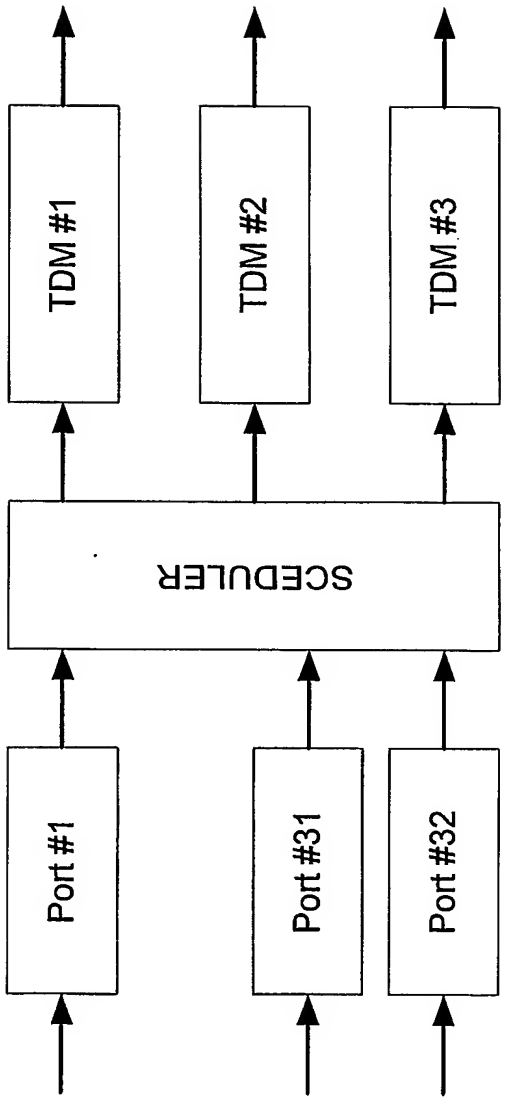


Figure 30 AMM 20p without redundant power distribution

31

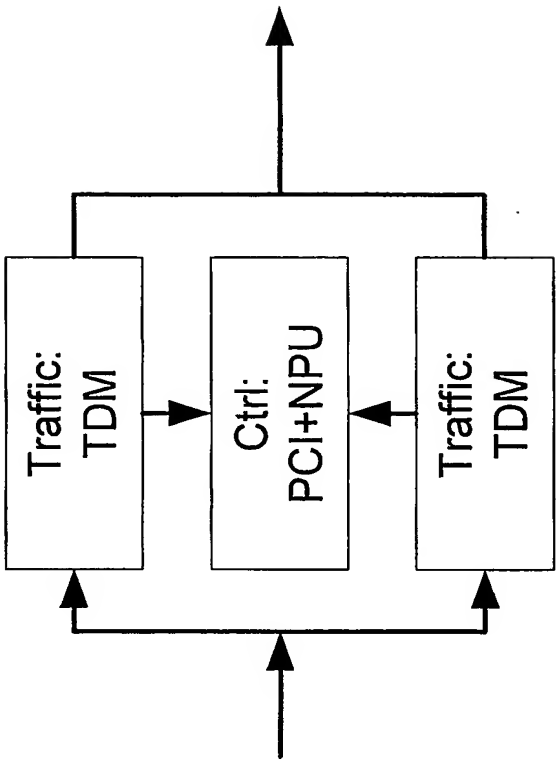


Figure 31 AMM 6p BN

32

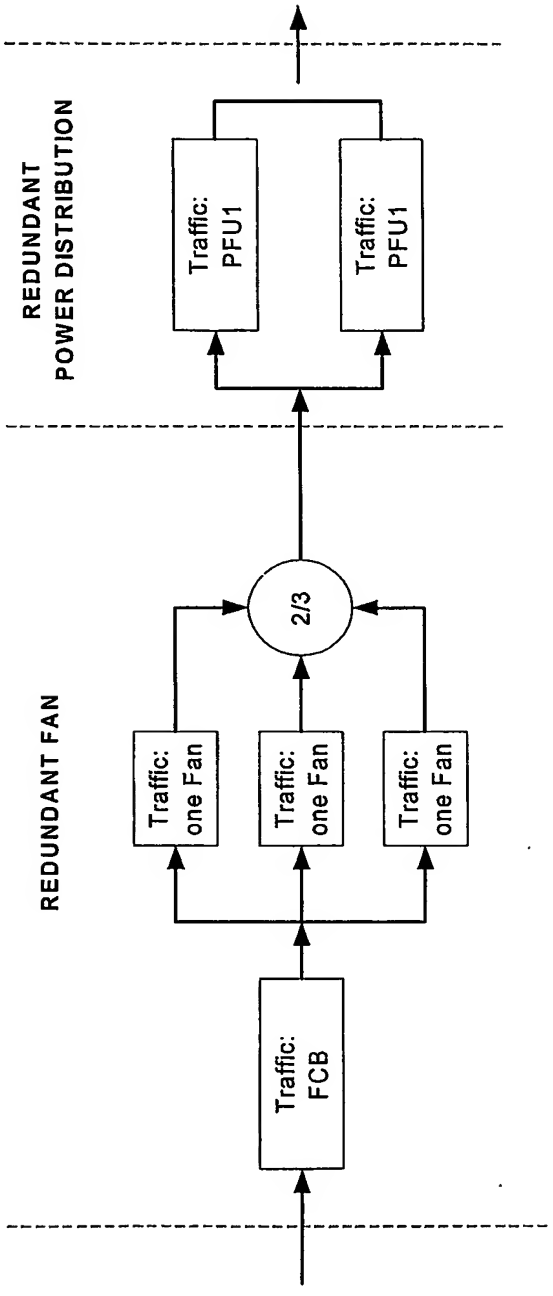


Figure 32 General model for protected interfaces

33

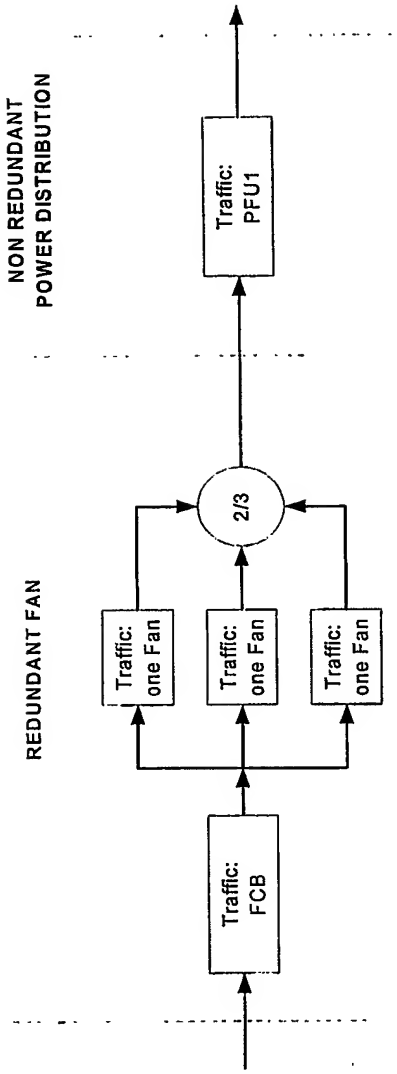


Figure 33 Simplified model for protected interfaces

34

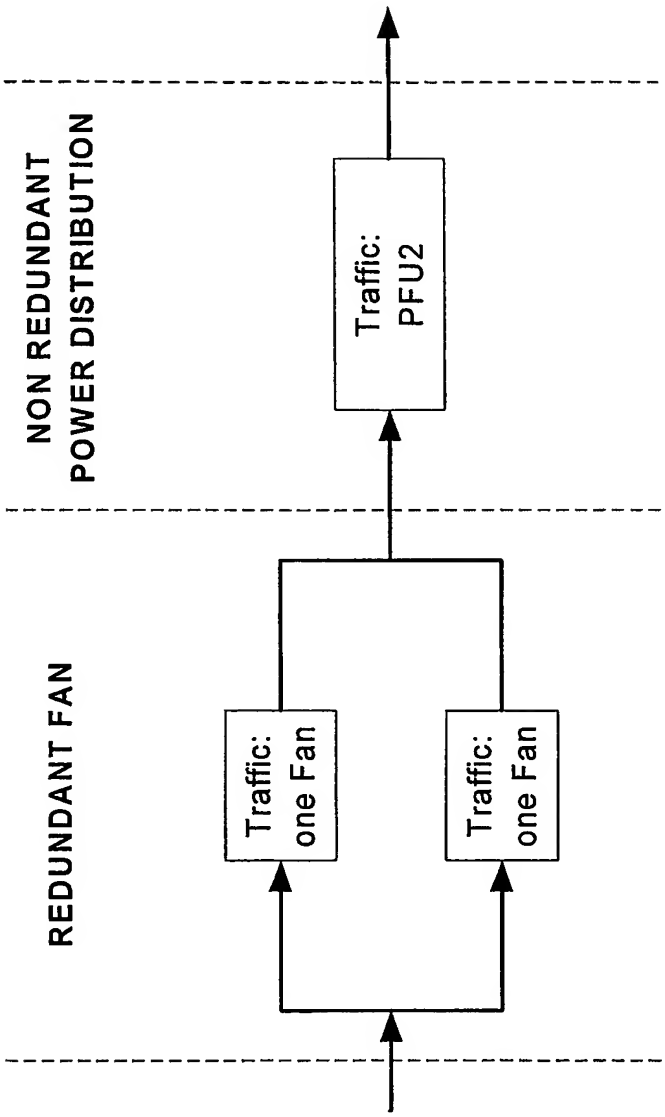


Figure 34 General model - unprotected interfaces

35

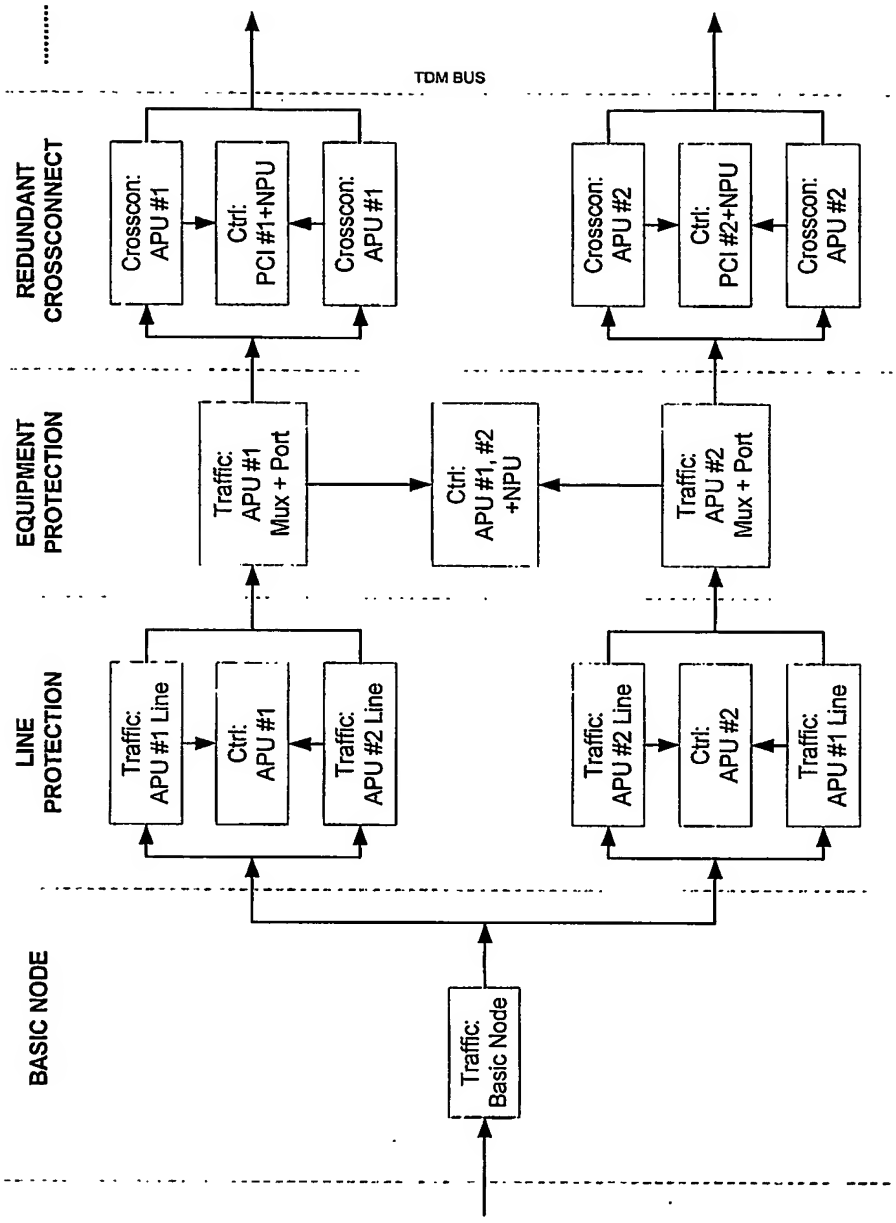


Figure 35 MCR 1+1

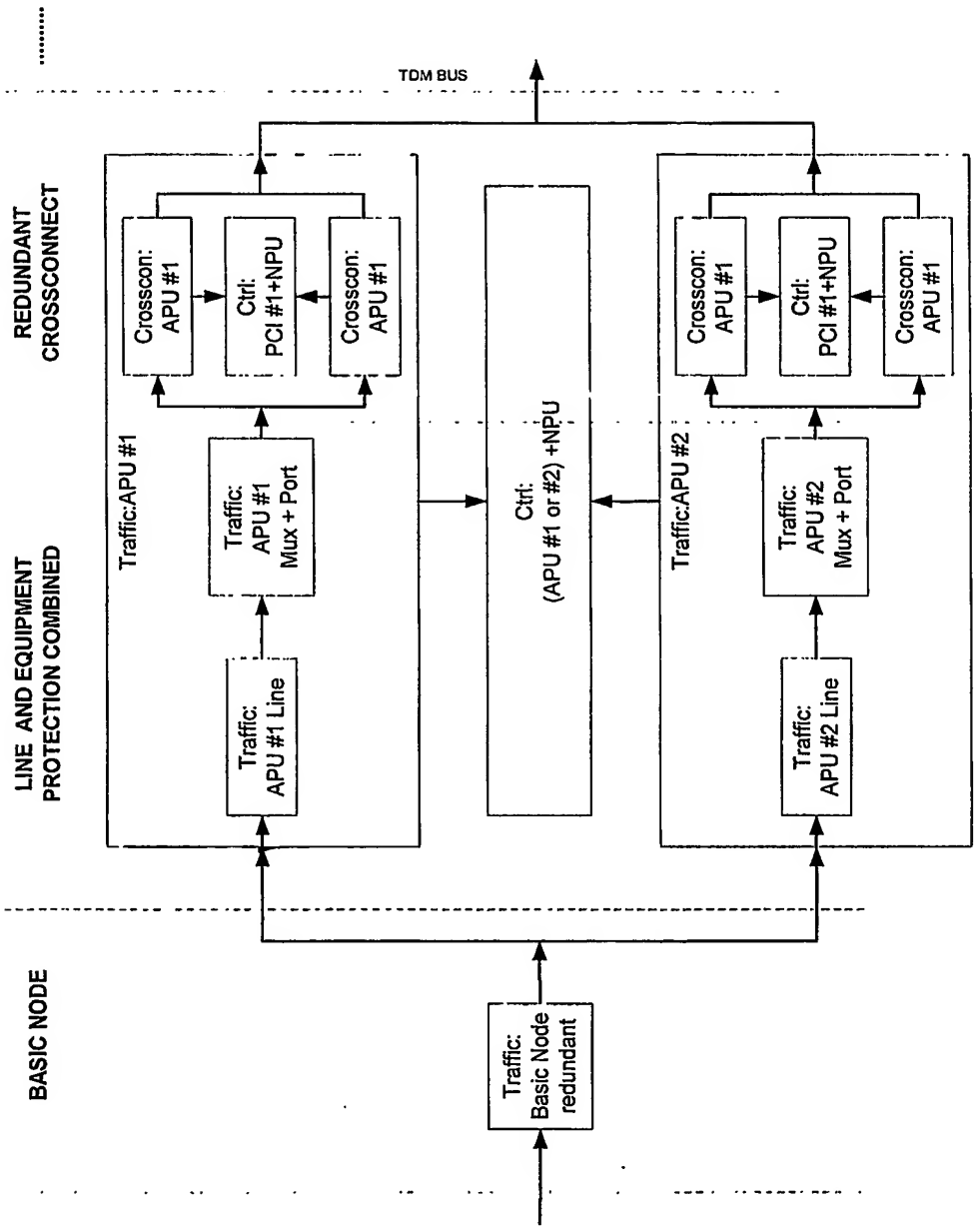
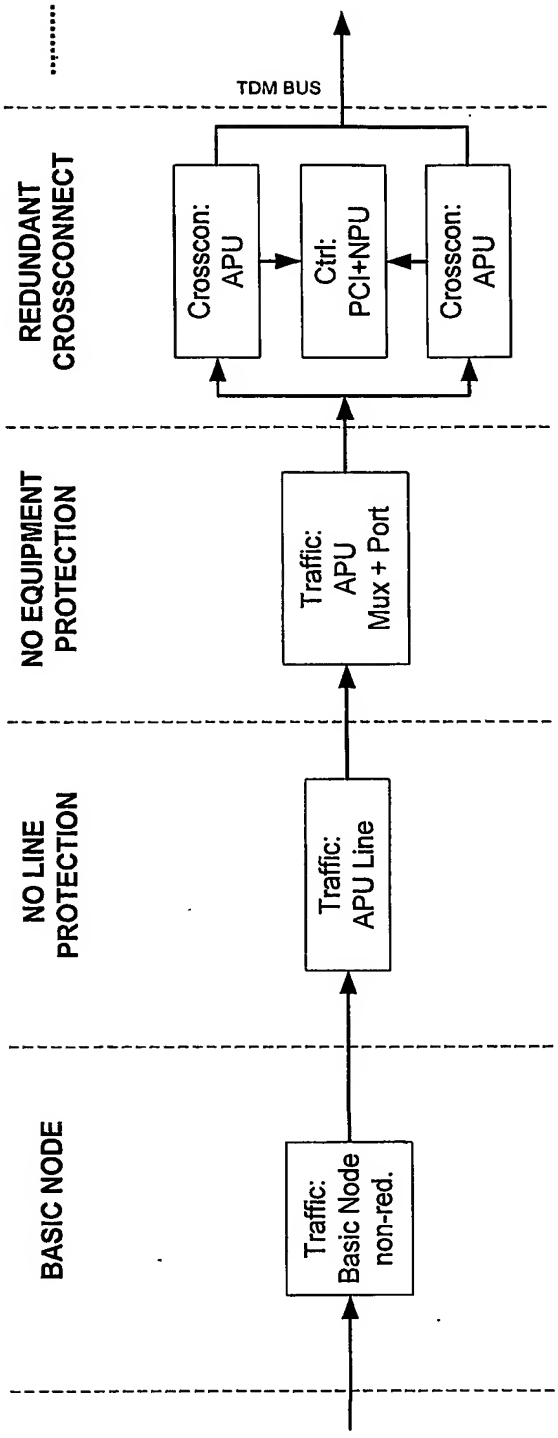


Figure 36 MCR 1+0



37

Figure 37 MCR terminal 1+1

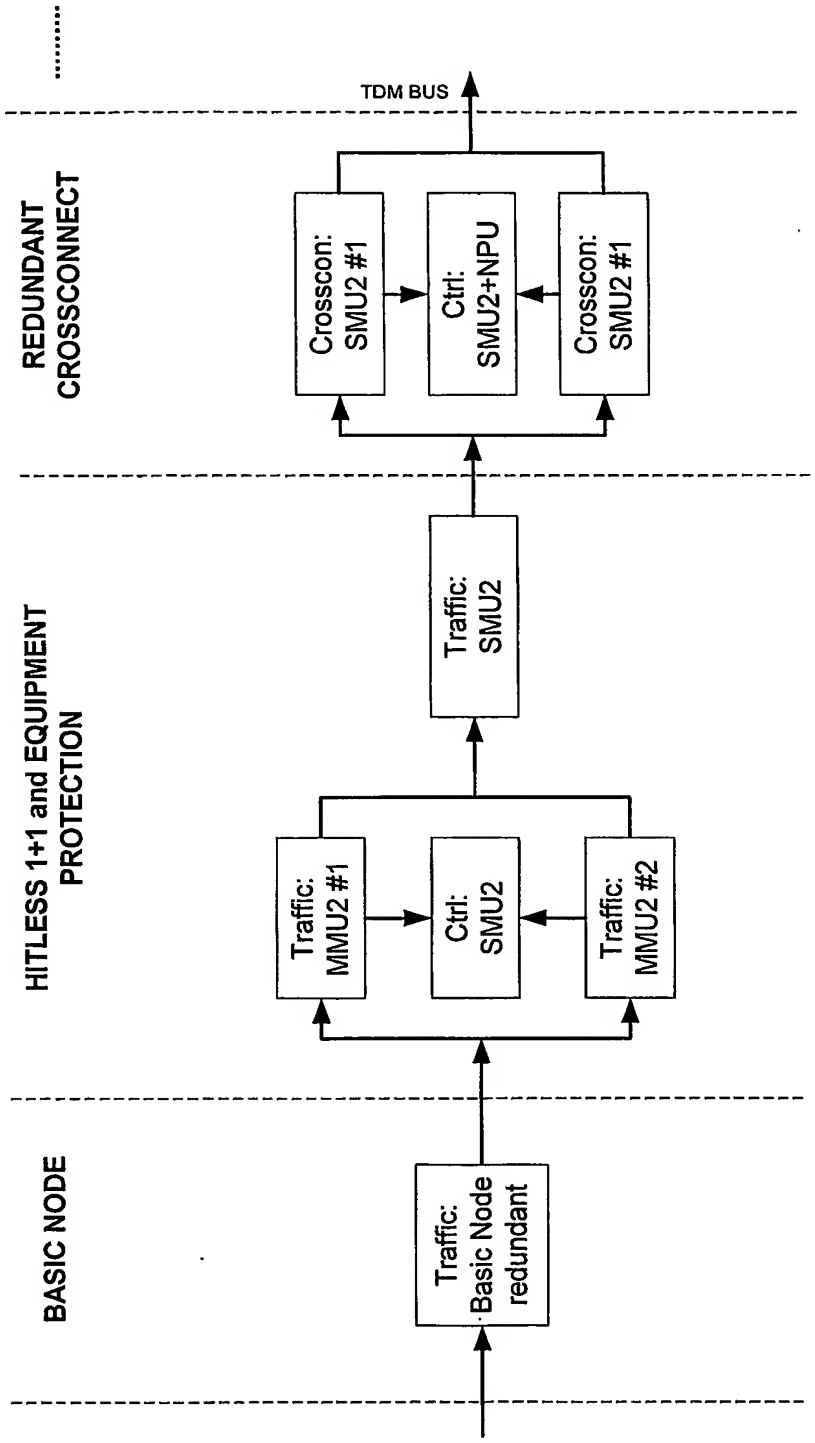


Figure 38 MCR terminal 1+0

38

39

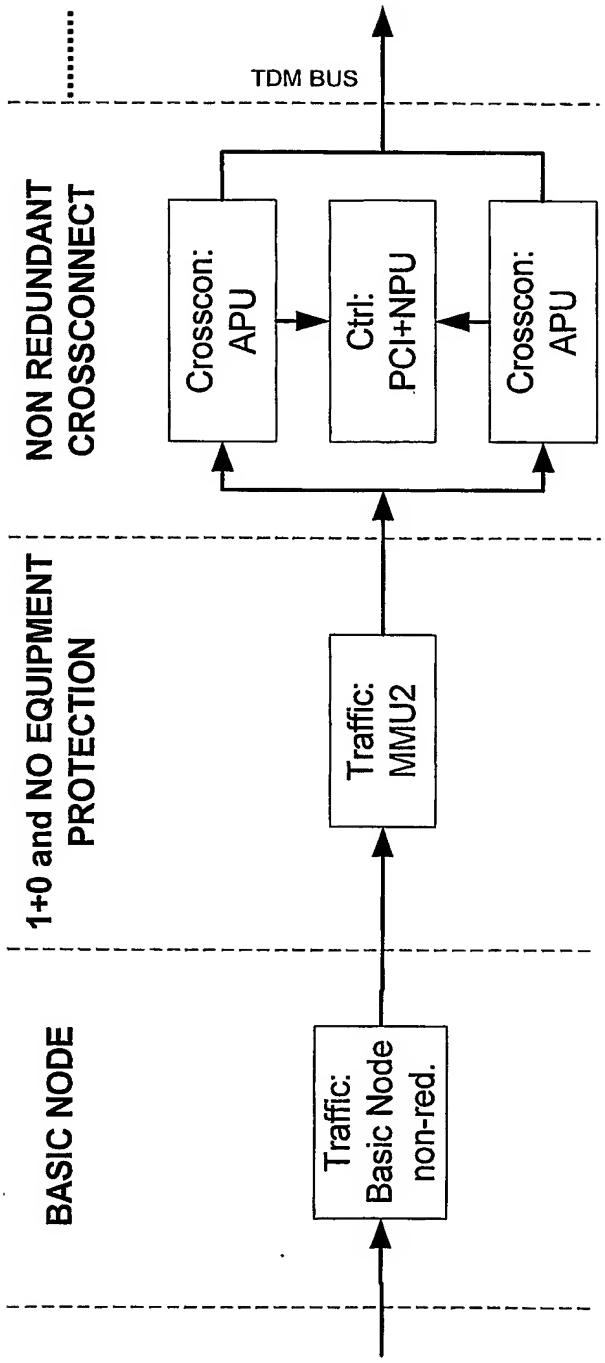


Figure 39 STM-1 terminal 1+1

40

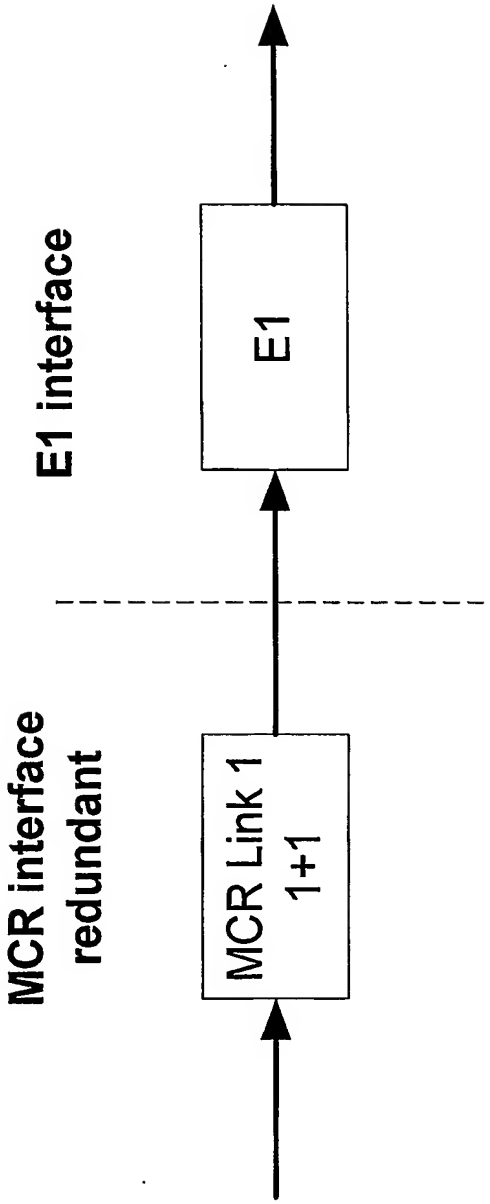


Figure 40 STM-1 terminal 1+0

41

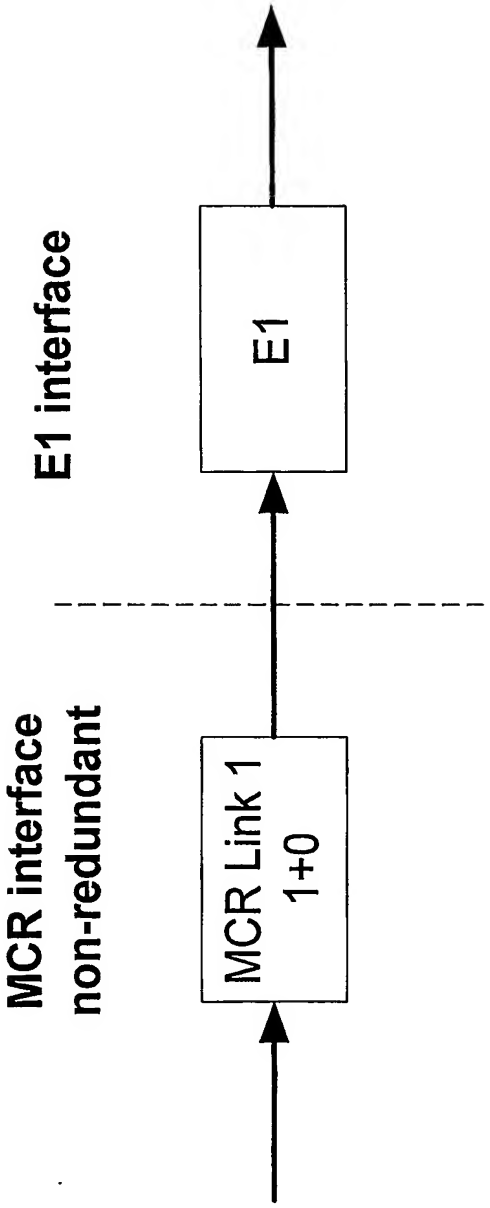


Figure 41 E1 terminal 1+1

42

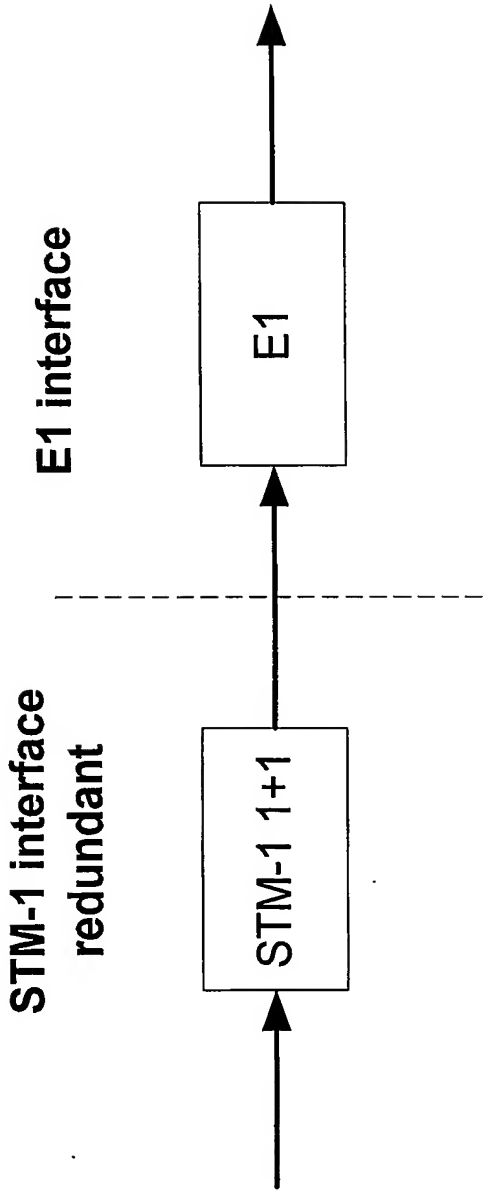


Figure 42 E1 terminal 1+0 (SNCP)

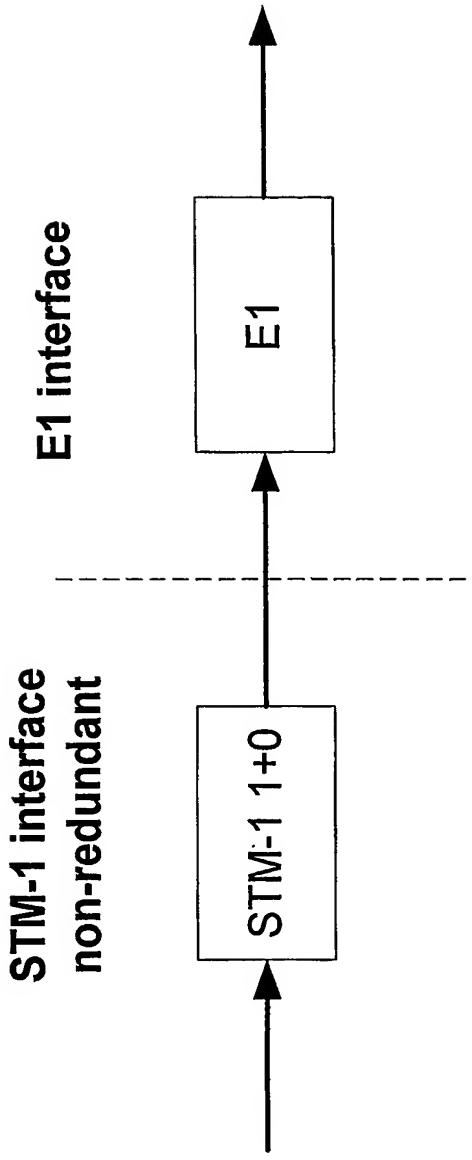


Figure 43 Install new node

44

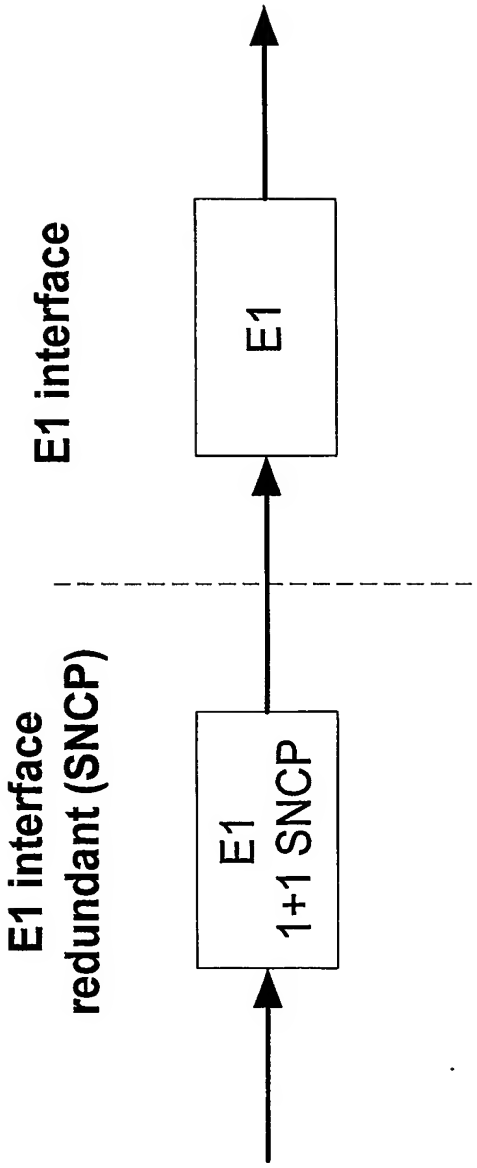


Figure 44 Repair NPU

45

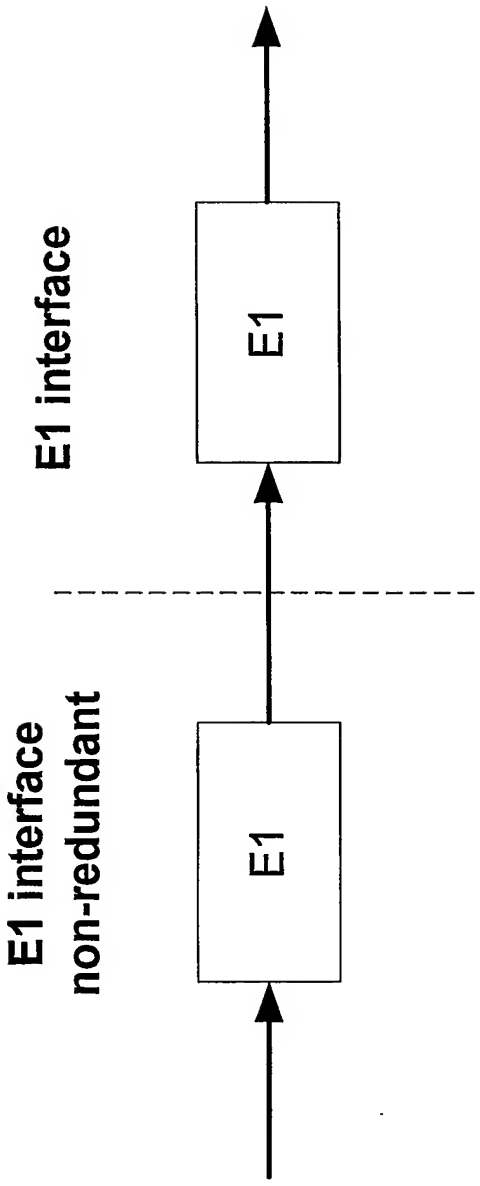


Figure 45 Change forgotten password

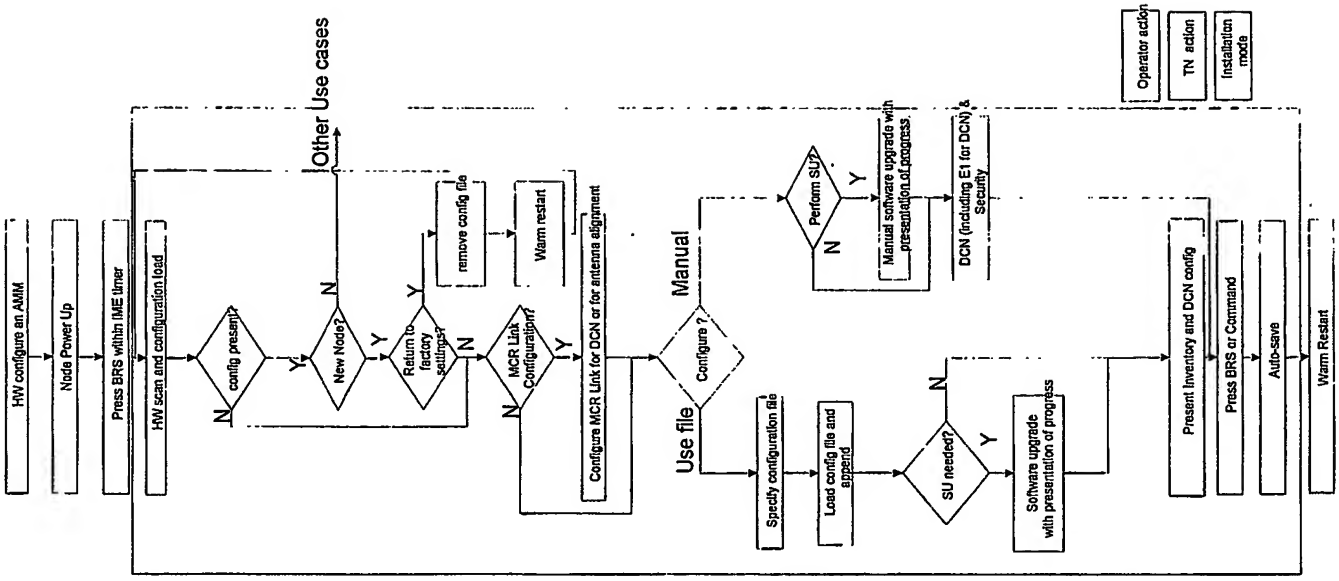


Figure 46
Emergency fallback NPU

46

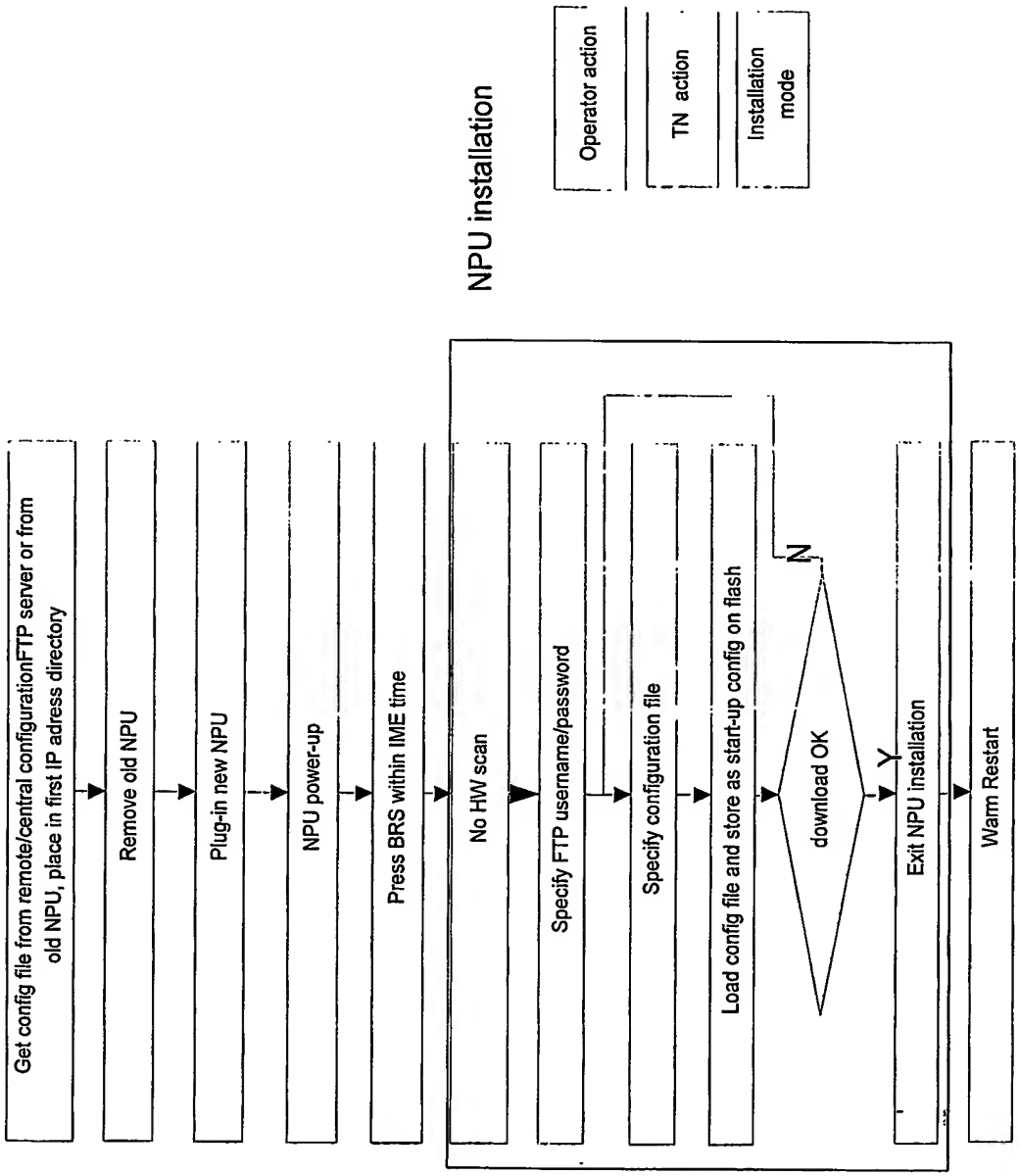


Figure 47 Removal of board (for information only)

47

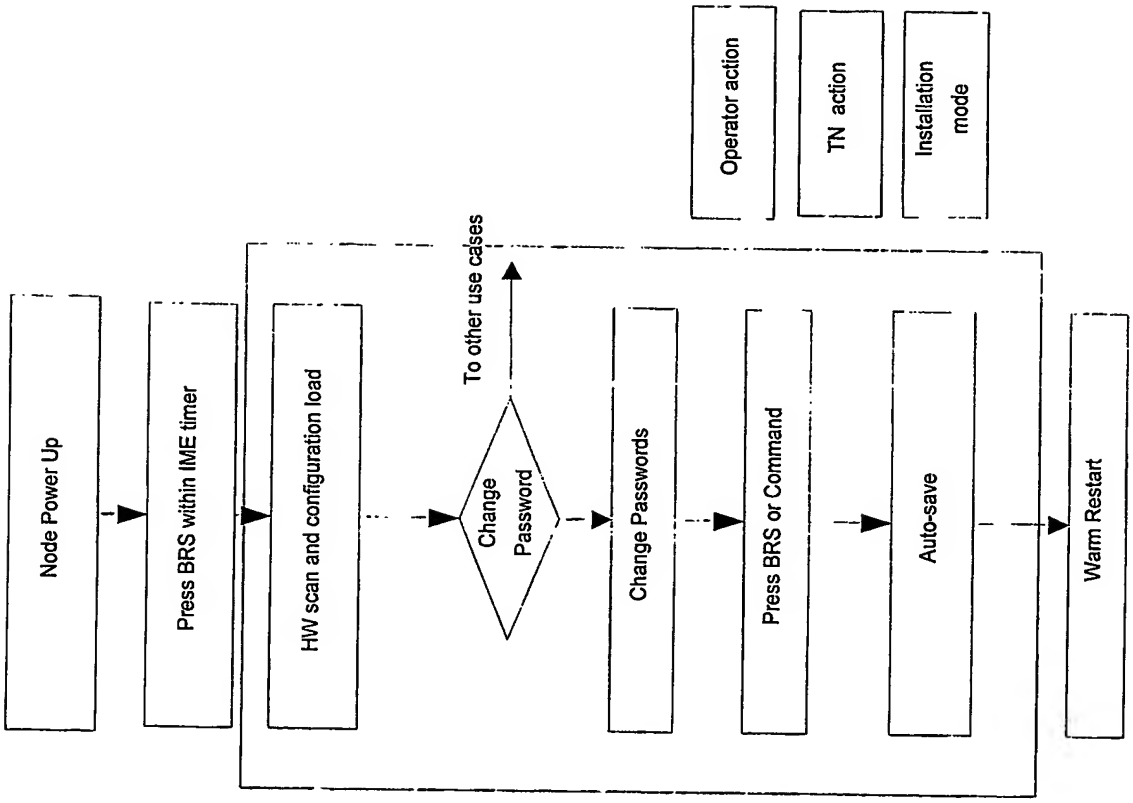


Figure 48 Fault handling of hardware and software error.

48

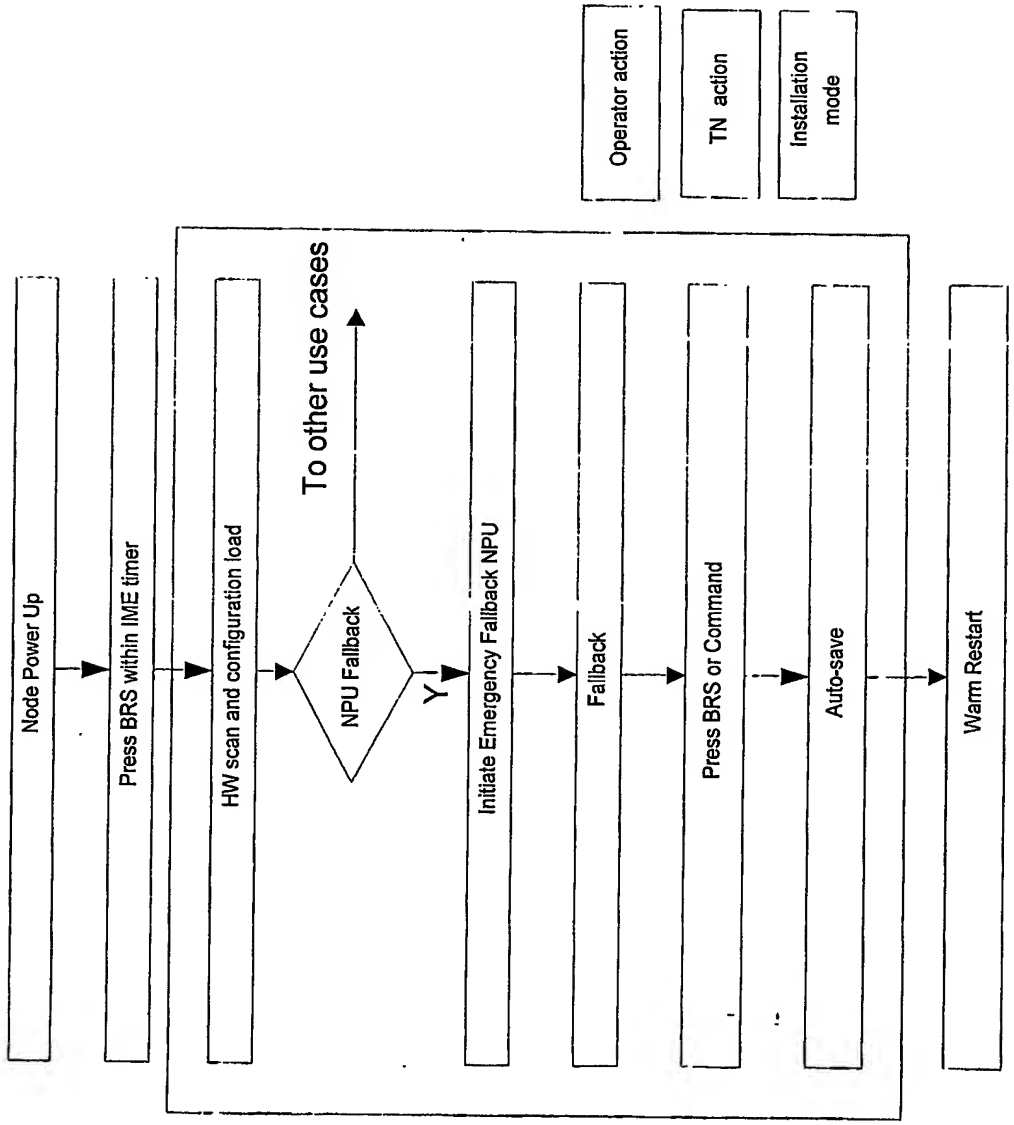


Figure 49 TN Handling of node error.

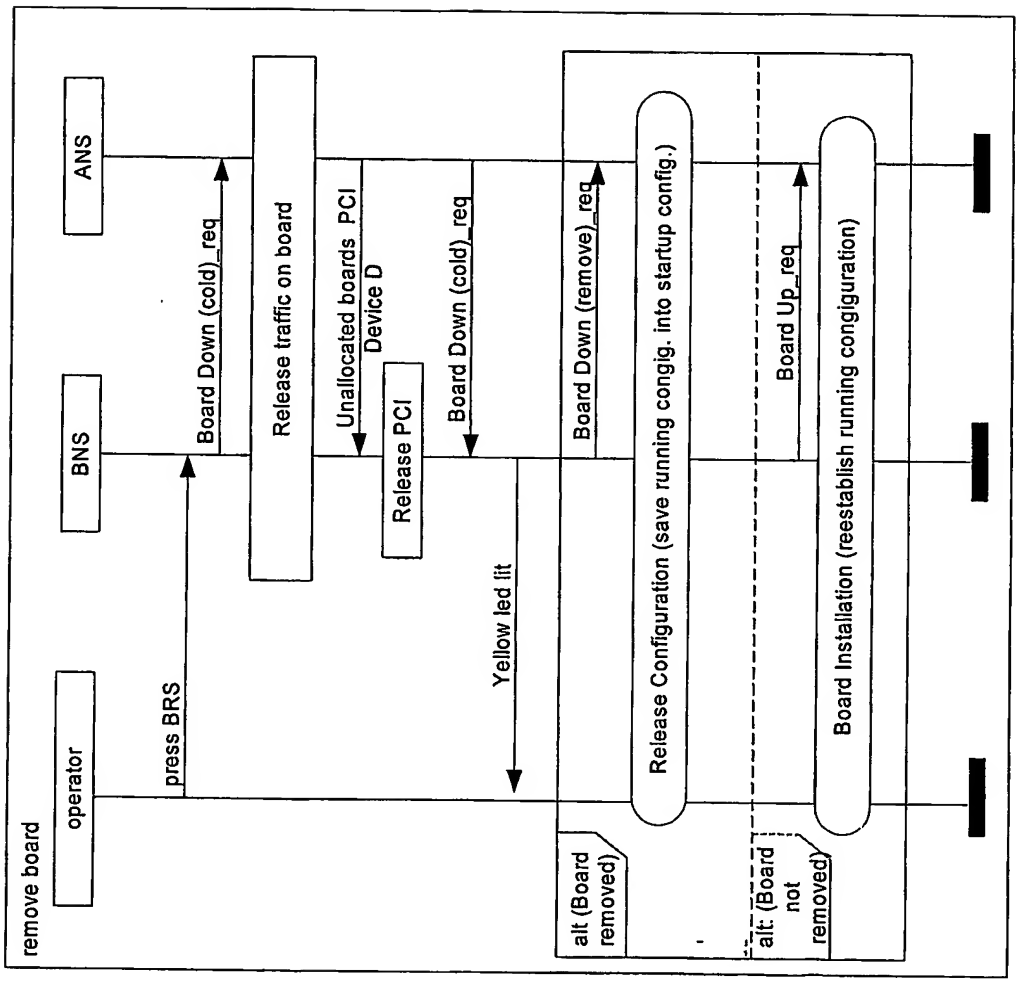


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Figure 50 TN Handling of APU/PIU errors.

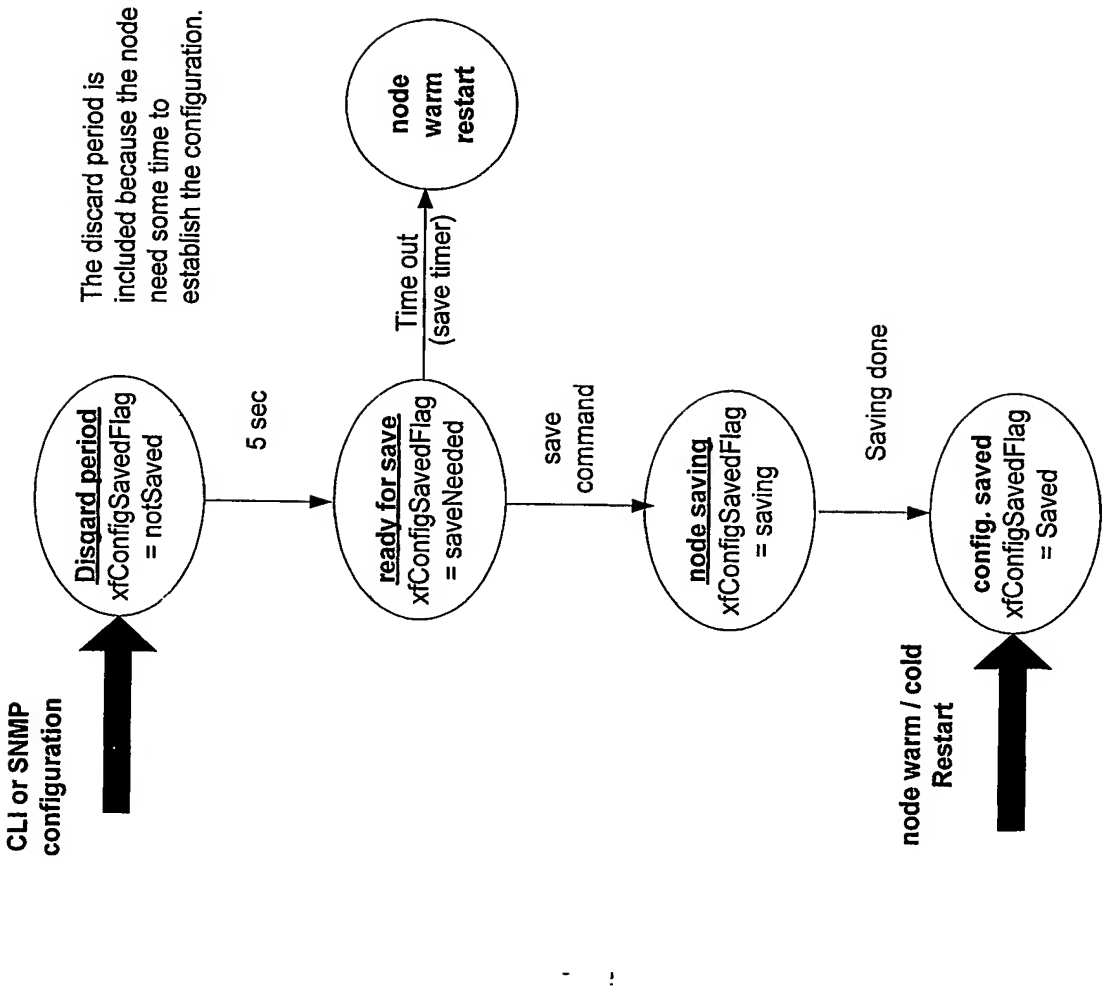

Figure 51 example of TN System Release structure

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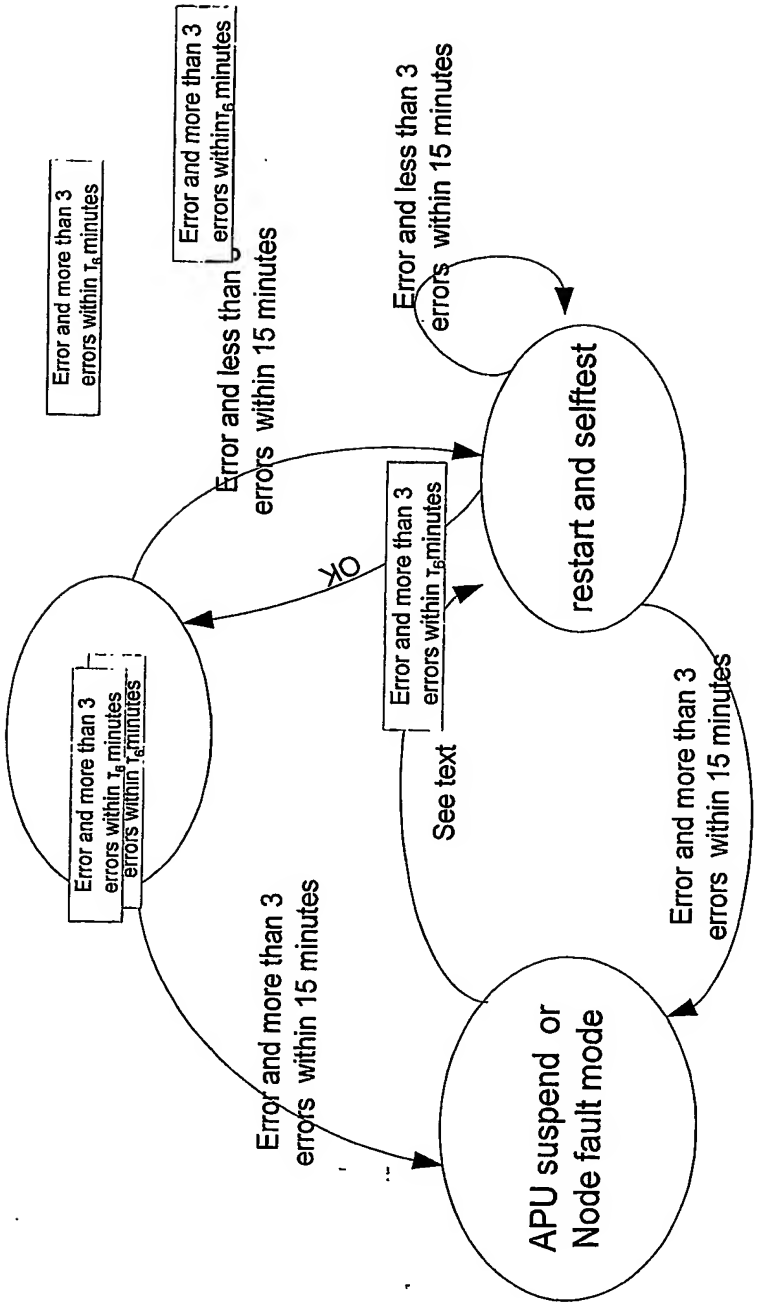

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Figure 52 Illustration of the various contents of the APU/NPU memory banks

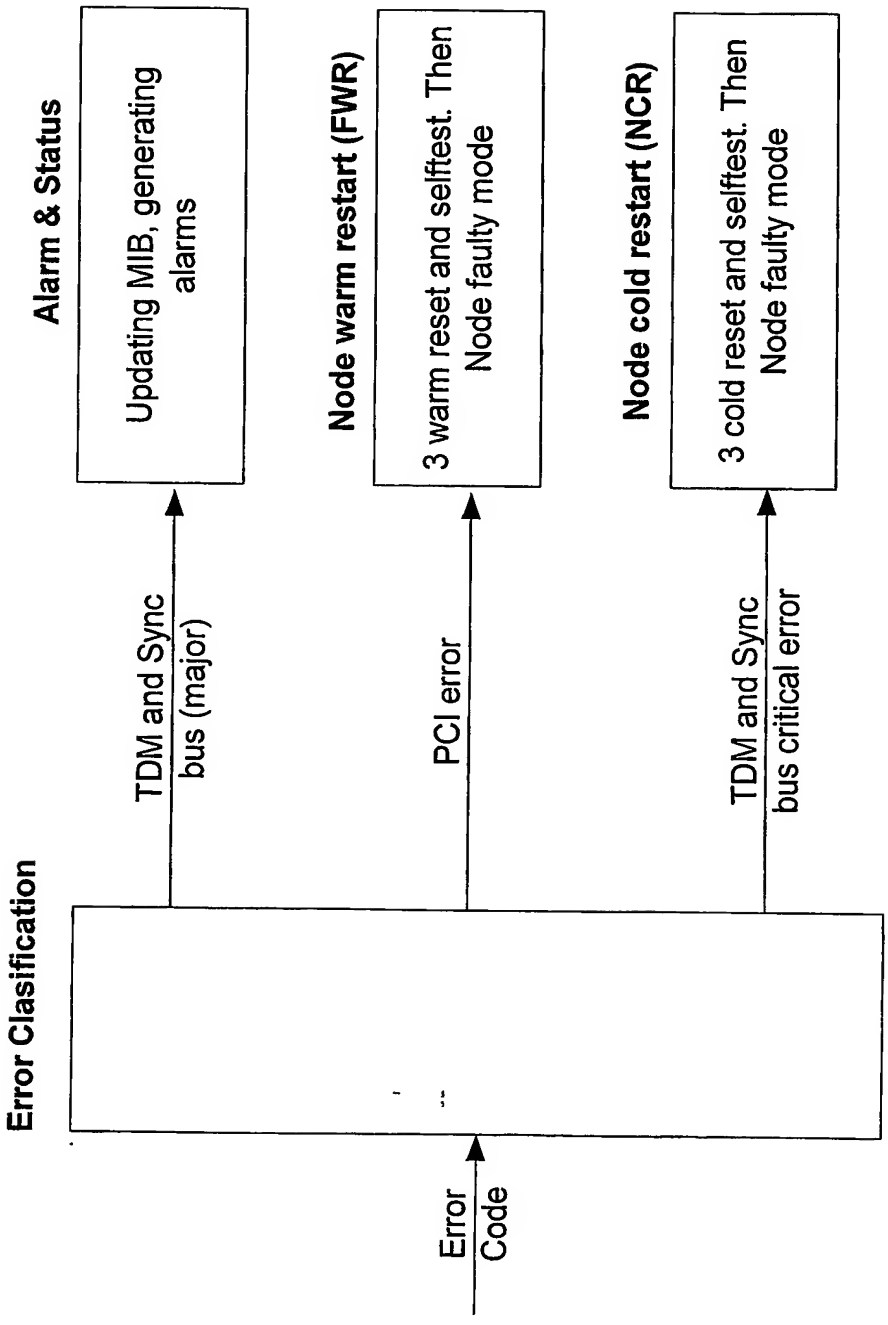


Figure 53 The Software Upgrade process illustrated

53

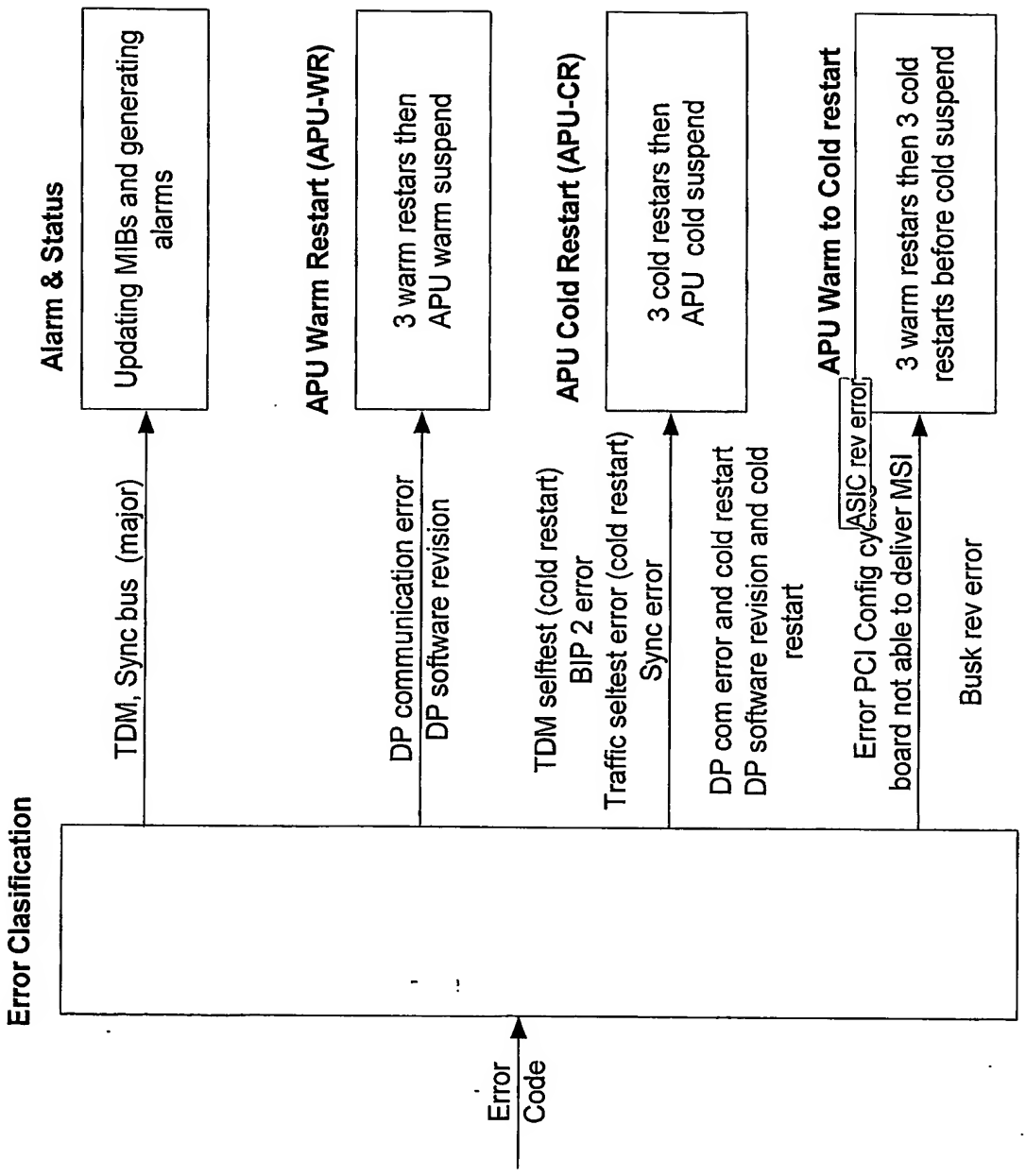


Figure 54 Su of a single APU due to a APU restart

54

55

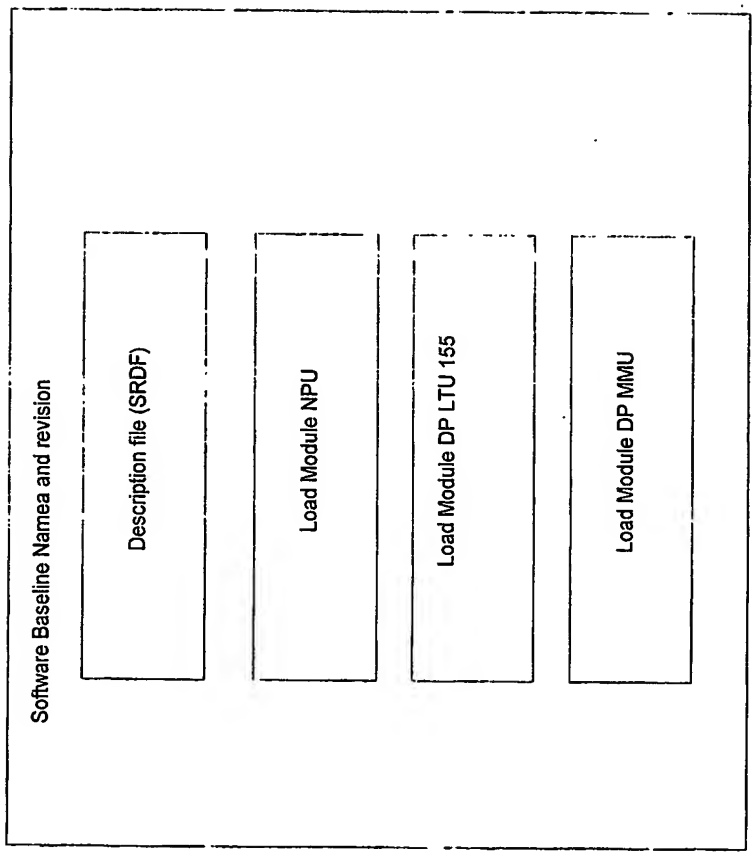
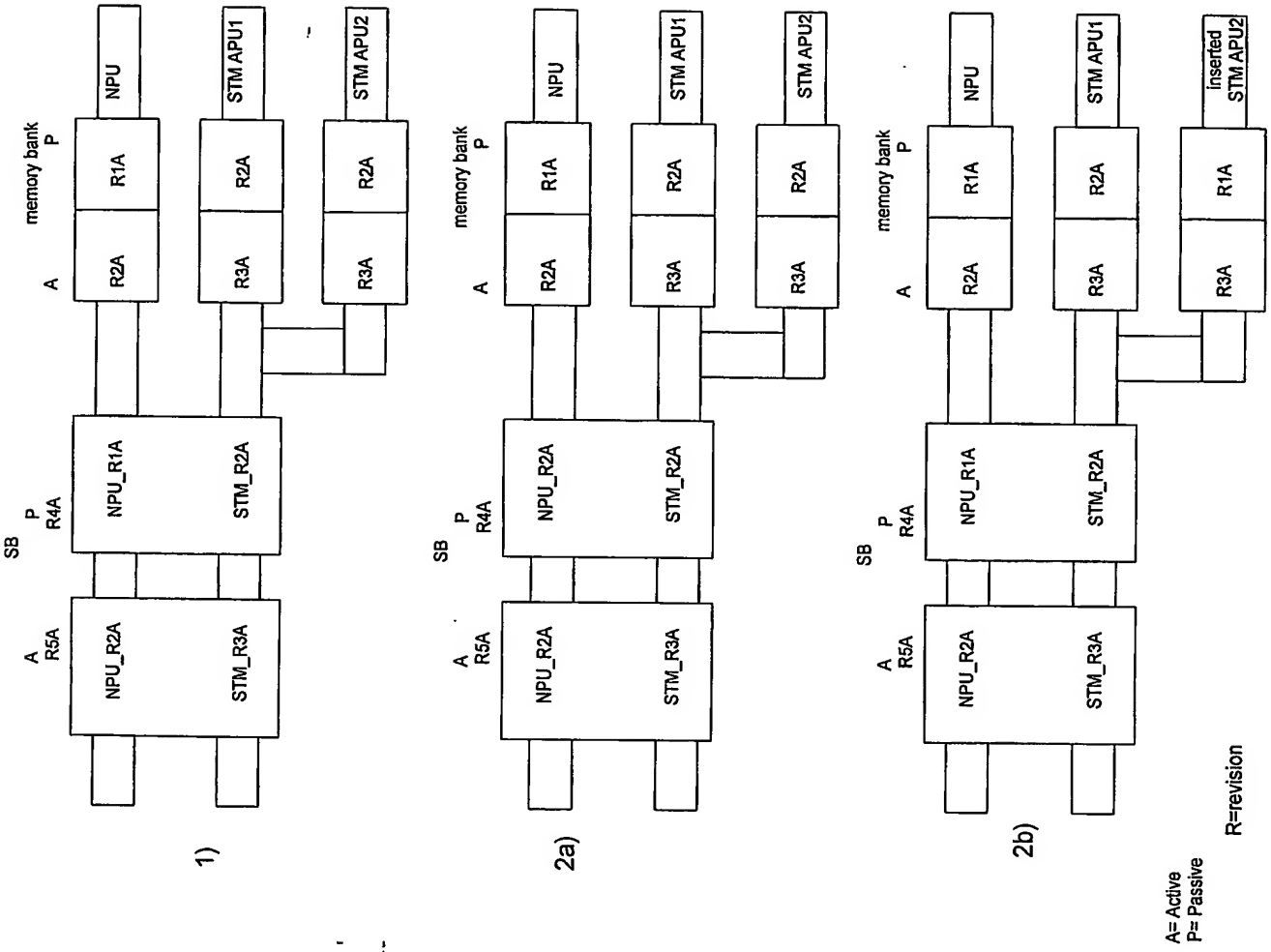


Figure 55 Hot Swap Software Upgrade


memory bank
SB
A
P
R5A
R4A
R2A
R1A
NPU_R2A
NPU_R1A
STM_R3A
STM_R2A
NPU
STM APU1
STM APU2
inserted STM APU2
1)
2a)
2b)
R=revision
A= Active
P= Passive

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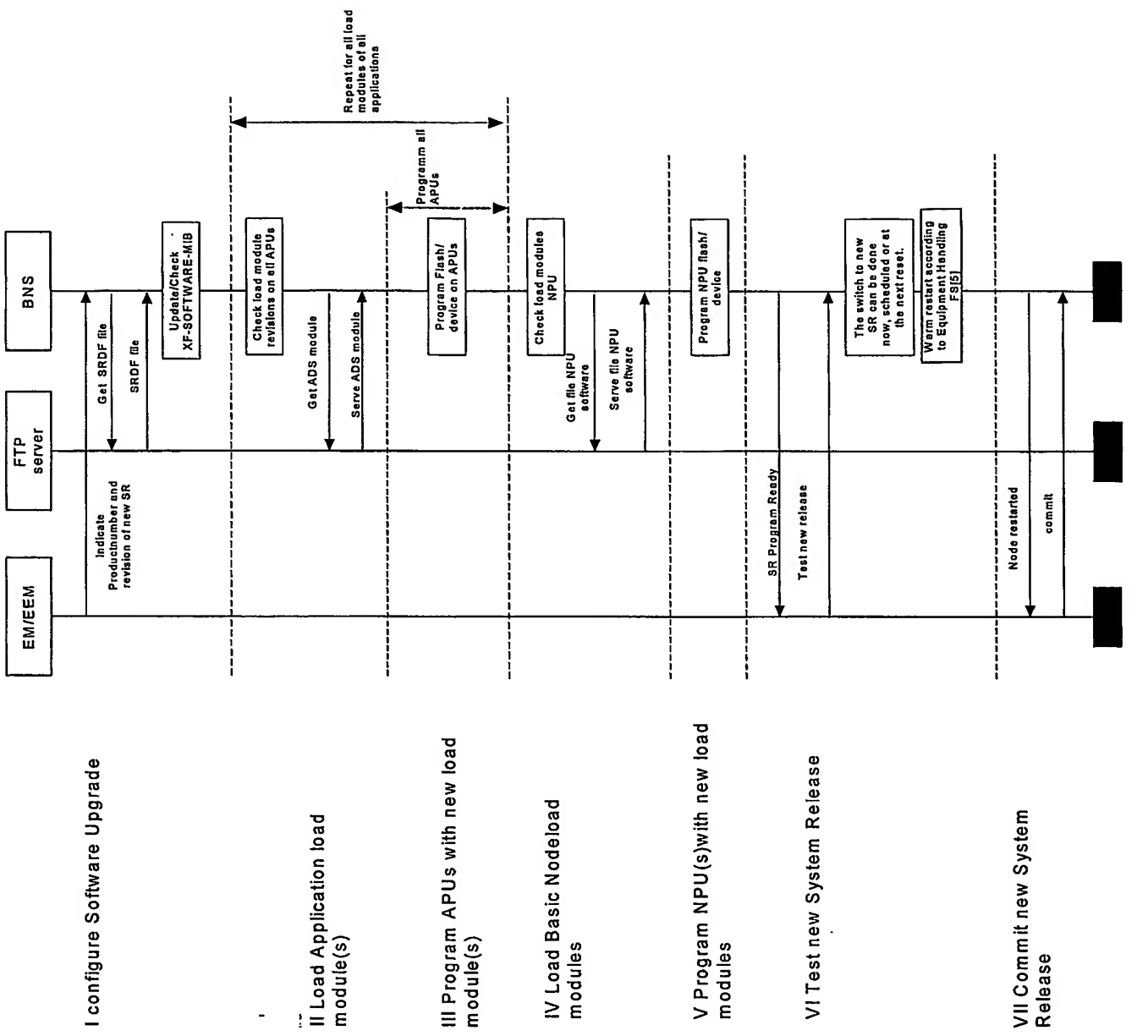
EM/EEM
FTP server
BNS
Indicate Productnumber and revision of new SR
Get SRDF file
SRDF file
Update/Check XF-SOFTWARE-MIB
Repeat for all load modules of all applications
Check load module revisions on all APUs
Get ADS module
Serve ADS module
Programm all APUs
Program Flash/ device on APUs
Check load modules NPU
Get file NPU software
Serve file NPU software
Program NPU flash/ device
SR Program Ready
Test new release
The switch to new SR can be done now, scheduled or at the next reset.
Warm restart according to Equipment Handling FS[5]
Node restarted
commit
I configure Software Upgrade
II Load Application load module(s)
III Program APUs with new load module(s)
IV Load Basic Nodeload modules
V Program NPU(s)with new load modules
VI Test new System Release
VII Commit new System Release

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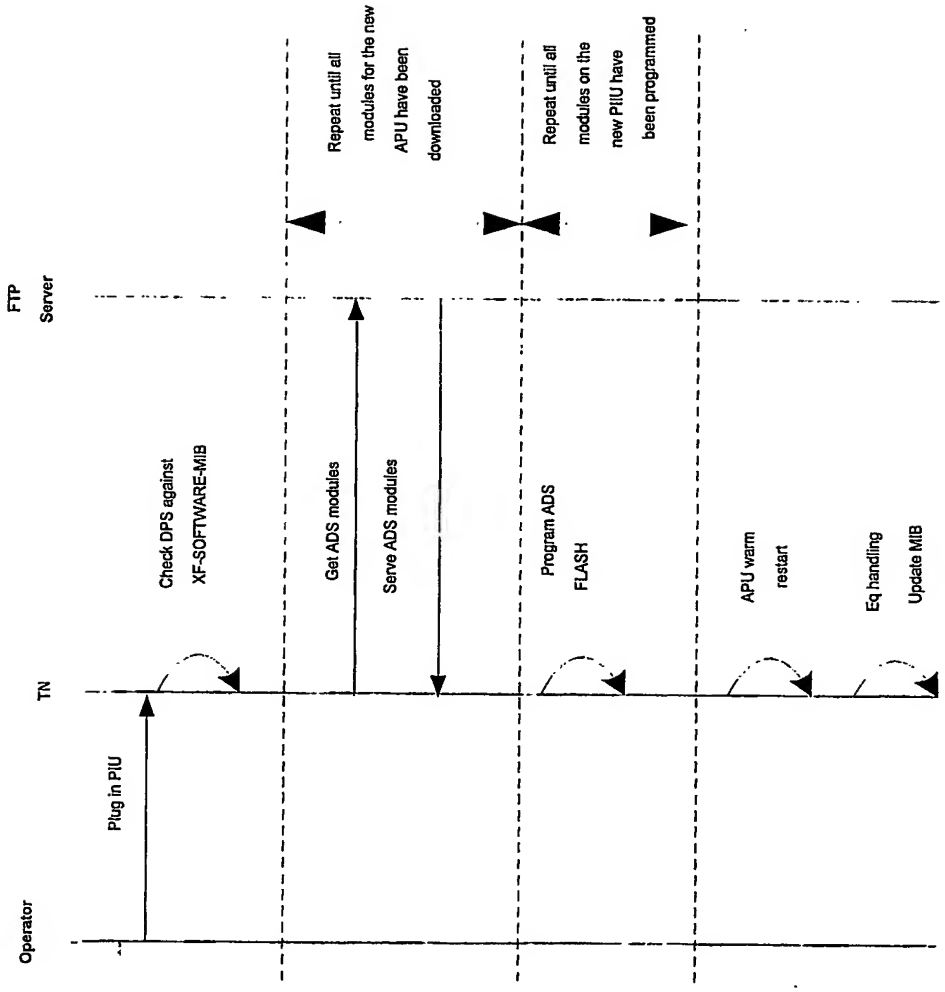
Operator
TN
FTP Server
Plug in PIU
Check DPS against XF-SOFTWARE-MIB
Get ADS modules
Serve ADS modules
Repeat until all modules for the new APU have been downloaded
Program ADS FLASH
Repeat until all modules on the new PtIU have been programmed
APU warm restart
Eq handling
Update MIB

Figure 58

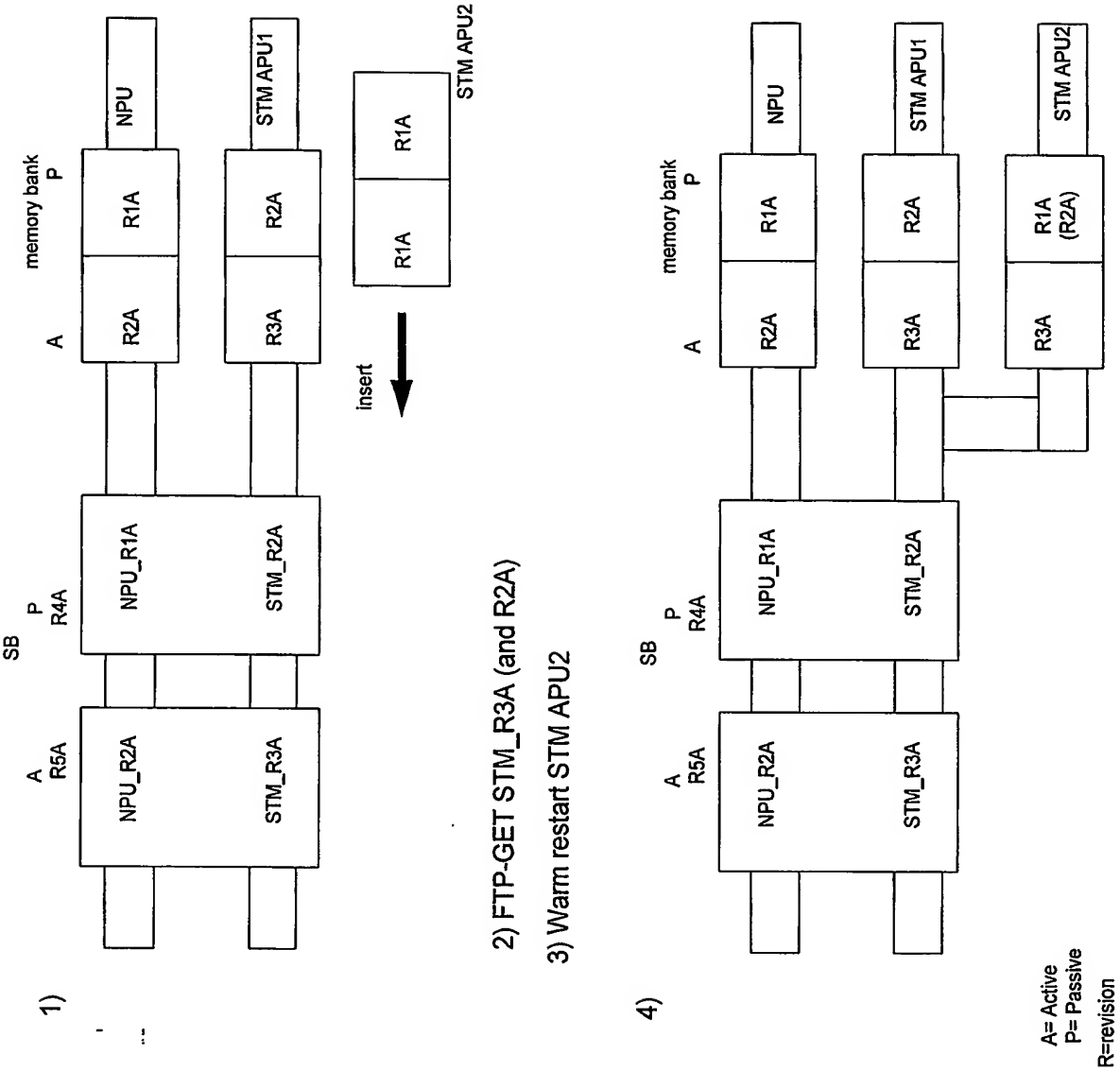
1)
SB
P
R4A
A
R5A
NPU_R1A
NPU_R2A
STM_R2A
STM_R3A
memory bank
P
A
R1A
R2A
R2A
R3A
NPU
STM APU1
insert
R1A
R1A
STM APU2
2) FTP-GET STM_R3A (and R2A)
3) Warm restart STM APU2
4)
SB
P
R4A
A
R5A
NPU_R1A
NPU_R2A
STM_R2A
STM_R3A
memory bank
P
A
R1A
R2A
R2A
R3A
R1A
(R2A)
R3A
NPU
STM APU1
STM APU2
A= Active
P= Passive
R=revision

Figure 59

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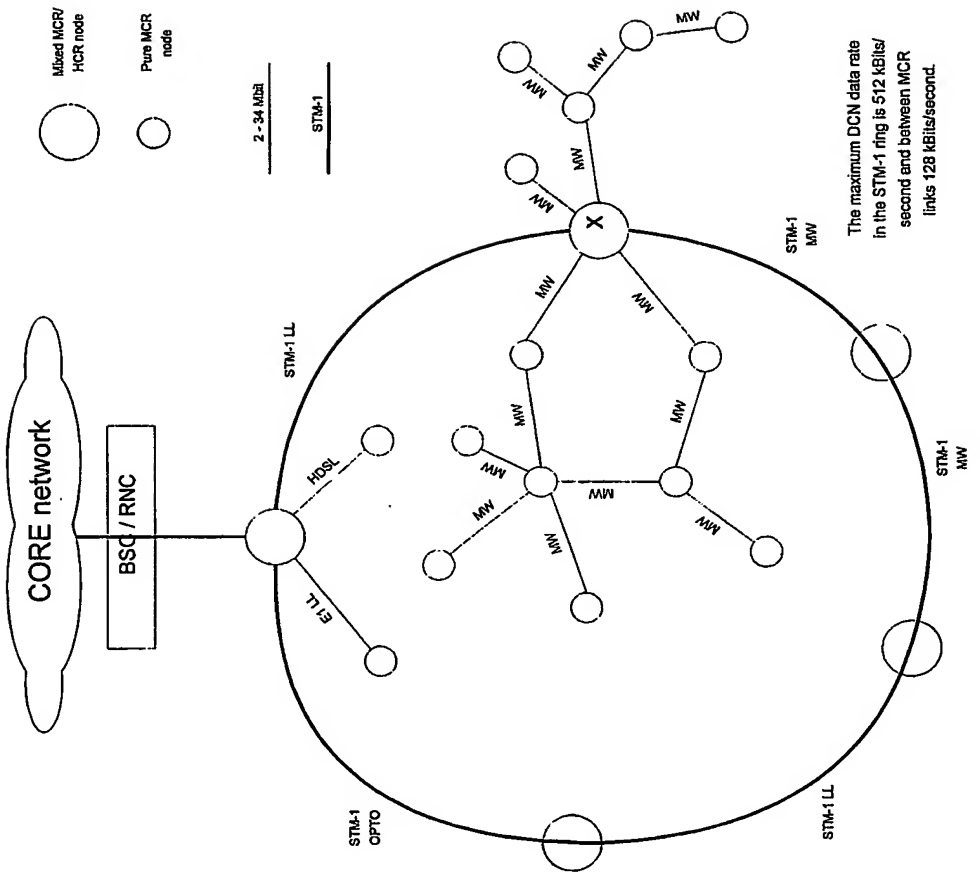
Mixed MCR/ HCR node
Pure MCR node
2 - 34 Mbit
STM-1
CORE network
BSC / RNC
HDSL
E1 LL
STM-1 LL
STM-1 OPTO
STM-1 LL
STM-1 MW
STM-1 MW
MW
The maximum DCN data rate in the STM-1 ring is 512 kBits/ second and between MCR links 128 kBits/second.

Figure 60

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